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Article

Adaptive Pulse-Controlled Learning in Differential 1T1R Memristor Crossbar for Neuromorphic Computing

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Abstract: Neuromorphic computing has been proposed as an exciting paradigm to accomplish energy-efficient artificial intelligence by replicating the working principles of biological neural networks. Here, the memristor has attracted a lot of interest because of its capability of mimicking the synaptic behavior by means of programmable conductance states. Nonetheless, traditional neural architectures using memristors have a few drawbacks such as low precision of weights, device variability and inefficient programming schemes that limit their direct application to large systems. The current work suggests a pulse-controlled learning scheme based on an adaptive pulse that is embedded into a differential 1T1R memristor crossbar design to improve the accuracy of programming synaptic weights and energy efficiency. The overall aim is to actively control the conductance of memristors with feedback-based pulse width modulation, which allows neural network weights to be mapped accurately, nonlinearity and drift effects to be reduced. The proposed design is a hybrid analog design that includes a parallel vector-matrix multiplication with a differential memristor crossbar, a pulse generation unit with adaptive programming and an analog front-end that includes a differential amplifier and comparator to process and activate signals. There is also a write-verify scheme which iteratively varies pulse width according to real-time measurements of conductance, which ensures that the weight values converge to desired values. The conductance update dynamics are modeled mathematically in order to optimize pulse parameters in order to enhance performance of learning. Simulation findings indicate that the proposed adaptive pulse-controlled strategy attains a higher weight programming precision, lower power usage, and a shorter convergence time than fixed-pulse technique. Moreover, the architecture has a better olerance to device variability, and can be used in scaleable implementations of neuromorphic hardware. These results indicate that adaptive pulse modulation is effective in supporting the future of memristor-based neural network designs in neural computing applications at the edge.

Keywords: — Neuromorphic Computing, Memristor, Differential 1T1R Crossbar, Adaptive Pulse Control, Pulse Width Modulation (PWM), Synaptic Weight Programming.

1. Introduction

Neuromorphic computing has become a groundbreaking paradigm, which seeks to imitate the effectiveness and parallelism of biological neural systems. As data-intensive applications like medical imaging, autonomous systems and edge intelligence continue to proliferate, there has been a growing need to have hardware efficient models that can execute complex processes such as segmentation and classification. Traditional CMOS-based architectures are powerful but have a high energy consumption and low scalability in the execution of deep neural networks. In this regard, memristor technology has received much attention because it has the ability to simulate synaptic behaviour as a result of programable conductance states. In-memory computation of arrays of crossbar memristor arrays can lead to a significant decrease in the data movement, which results in a more efficient computation [1]. This is especially critical to segmentation and classification tasks, which demand large-scale operations on matrices and real-time processing. Memristor-based systems have a potential to be a solution to future generations of hardware used in artificial intelligence by combining memory and computation on the same physical device. This has made the investigation of effective architectures which exploit memristors in their segmentation and classification a pressing research direction.

The tasks of segmentation and classification are commonly tackled through a deep learning framework where convolutional neural networks (CNNs), encoder-decoder frameworks, and transformer-based models are used. Commonly used structures in segmentation models include U-Net, fully convolutional networks (FCNs), or attention-based mechanisms to extract spatial and contextual information about input data. The prediction of interest areas is accurately demarcated by these models as they do pixel-level predictions. On the other hand, classification models learn to discriminate features to classify input samples, often by using fully connected layers or global pooling. Classification models are reduced in hardware-based models to the form of accelerators which can perform fast vector-matrix multiplications. This has been commonly achieved using memristor-based crossbar arrays that are capable of performing parallel analog operations based upon Ohm's and Kirchhoff's laws. Moreover, methods such as the differential conductance encoding, analog-digital interfacing and analog-digital hybrid processing are typically used to enhance precision and robustness. The learning techniques include off-line learning where weight transfer is employed or in-situ learning where adaptive learning schemes are used [2].

The current segmentation and classification methods have shown that they have significantly improved their accuracy, throughput and speed. Deep learning segmentation techniques are extremely precise to detect complex patterns, especially for biomedical image processing and object detection. Similarly, classification models have been effective in the determination of features in various data sets. They have reduced latency and reduced power usage, when implemented on memristor-based hardware, when in parallel in-memory computation is desired. These systems have been discovered to be useful in edge applications because research has documented throughput and energy efficiency gains on traditional digital processors. Differential crossbar architectures have also been used to achieve robustness through the minimization of noise and maximization of signal integrity. The adaptive programming methods have been employed too in the enhancement of the weight tuning and acceleration of convergence in the training process. Overall, these advances prove that there is a favorable trend towards efficient hardware-software co-design where memristor-based hardware is significant in accelerating the segmentation and classification of data without competitive advantage [3].

Although this is a giant leap, there are minor challenges to the adoption of the memristor based segmentation and classification systems. The most conspicuous issue is the inconsistencies between devices and consequently variability in the conductance states affecting the accuracy of calculations. Even the weight programming can be regarded as a challenging task due to the imprecision of the weight and the nonlinear switching behavior. In addition, sneak path currents in large arrays of crossbar may result in errors during read and write operations [4]. Systemwise, mapping of complex deep learning models to hardware is to be done with a lot of care so that a trade-off between accuracy and efficiency can be made. Analog noise, absence of dynamic range and the problems of interfacing between analog and digital components also influence performance. Moreover, it is still challenging to train memristor-based networks in real time as there are no accurate and stable programming schemes. Although hybrid methods can be used to alleviate these problems, they tend to add to the complexity. These shortcomings demonstrate the necessity of better programming schemes, strong architectures, and adaptive learning systems to maximise the potential of neuromorphic systems based on memristors [5].

This paper presents a pulse gated memristor based artificial neural network architecture, which will be effective in segmentation and classification of data. The suggested approach uses the difference between conductance of a memristor crossbar array to encode the synaptic weights with a 1T1R array, which allows the

positive and negative weights to be encoded correctly. One of the most important inventions is the combination of an adaptive pulse-width modulation scheme with a write verify scheme, which dynamically controls programming pulses in response to real time feedback to provide accurate conductance tuning. The method is useful in addressing device nonlinearity, variability as well as drift which are typical issues in memristor systems. The architecture enables parallel vector-matrix multiplication to achieve high-speed inference to suit computationally expensive tasks in segmentation, and is also able to sustain efficient classification. Also, analog front-end components like comparators and differential amplifiers can be included allowing powerful signal processing and activation. With a combination of device level optimization and system level ANN mapping, the technique proposed will increase the accuracy of the programming as well as minimize the power consumption and increase the scalability. This renders it an attractive option to the next-generation neuromorphic hardware that is expected to be deployed in edge intelligence applications.

The remainder of this paper is organized as follows: Section II reviews related existing work. Section III presents the mathematical modeling and analysis of the proposed memristor. Section IV discusses simulation results and their implications. Finally, Section V concludes the study.

2. Literature Survey

Creating r-simplicial sequence of different conductance values Alex and Leon propose a way to improve the resolution to build a super-resolution memristor crossbar with nodes made up of multiple memristors. The more the conductance values, the greater the range and the better the resolution of the crossbar. This is particularly useful in designing analog neural network (ANN) layers, which are known to be one of the most common ways of creating a neural network layer for neuromorphic computing [6]. Truong present a new architecture of memristor crossbar with bipolar inputs for image recognition. The proposed bipolar crossbar array is based on the simplified Exclusive-NOR, which is the basis of the operations of the bipolar crossbar array to determine the matching between the input pattern and the stored patterns. This new architecture uses only one crossbar array as opposed to two crossbar arrays. The proposed architecture has half the number of memristors of complementary and twin architecture. The proposed crossbar architecture that has bipolar inputs consumes 16.7% and 7.2% of the power consumed by complementary and twin architectures respectively. Also, using the proposed design, it is possible to use a single crossbar to increase the fault tolerance of a crossbar circuit [7].

Hanrui et al. presents a new low-power and efficient event-driven system for processing ECG signals using the memristors. It has a memristor-based level-crossing event encoder, and the design reduces redundant data to 88.23% of that in the traditional Nyquist sampling methods. It also introduces a cascaded memristor-based reservoir layer to process the event streams in real-time, and to map the temporal patterns to a high-dimensional feature space for efficient feature extraction. Matrix multiplication can also be accelerated by Crossbar array of memristor in classification of neuromorphic networks [8]. A real time classification of cardiac arrhythmia is proposed by Hassan et al. using memristor neuro morphic computing system to classify 5 beat types. Memristors are novel devices that are adopted in the neuromorphic computing systems. Hence, they provide a good balance between real time operation, power consumption and the accuracy of the system. The experiment results have shown that the proposed system is superior to most of the compared methods in terms of accuracy and testing time, as the average accuracy of the proposed system is 96.17% with the average testing time of 34 ms per beat [9].

Xiaoyuan et al. proposes a novel reservoir layer compromised of non-volatile memristor is designed to implement the reservoir computing (RC) system in which the reservoir states are calculated by the voltage across two memristors. This structure can easily nonlinearly map the one-dimensional voltage input signal to a two-dimensional space, thus, reducing the complexity of data analysis and enhancing the separability of the signal features, satisfying the requirement of RC of the high-dimension feature. The experimental results of the proposed RC system on electrocardiogram (ECG) classification task are the high classification accuracy of 98.3 percent and 100 percent of QRS complexes with and without shift, respectively which indicates the effectiveness of the proposed RC system [10].

These limitations are overcome in the proposed work by proposing an adaptive pulse-controlled learning mechanism in a differential 1T1R memristor crossbar architecture. This design, unlike the previous circuit-based designs, allows the synaptic weight to be programmed more accurately due to feedback-based pulse modulation, which enhances convergence, robustness, and energy efficiency. The proposed approach, combining device-level optimization with the implementation of system-level ANNs, addresses the gap between neuromorphic computing and memristor-based hardware.

3. Proposed Methodology

The suggested system, as shown in Fig. 1, introduces a differential 1T1R memristor crossbar-based architecture to perform artificial neural network (ANN) computation with a higher level of precision and a reduced energy consumption. The figure is divided into three levels that are interrelated, i.e. (a) ANN representation, (b) differential memristor crossbar implementation, and (c) 1T1R device structure. The main aim of this architecture is to support in-memory computing by combining storage and computation into a single physical architecture, which has surpassed the drawbacks of traditional von Neumann systems. At the top of the hierarchy, we have three basic elements: (i) ANN abstraction layer, (ii) differential memristor crossbar array, and (iii) 1T1R memristor cell structure. The ANN model describes the computational structure in which the input nodes are linked to the output neurons by weighted synaptic links. These weights are physically overlaid on the conductance states of memristors in the crossbar array. The differential crossbar design represents each synaptic weight with two memristors (G+,G−), which enable the representation of both positive and negative weights. The input voltages applied over the word lines (rows) are multiplied by the corresponding conductance values creating currents along the bit lines (columns). The addition of these currents is a natural consequence of Kirchhoff Current Law, which allows parallel multiplication of vectors and matrices (VMM), the fundamental calculation of ANN inference. The crossbar is made up of 1T1R cells, with a memristor in series with an NMOS transistor at each intersection. The transistor is an access device that is driven by the word line and provides selective read/write access and removes sneak path currents. The memristor is a memristive device that stores the weight information in the form of resistance states, which can be programmed using external programming pulses. The system is highly parallel in nature and several inputs are handled in parallel across the crossbar. Differential sensing circuits evaluate the difference between matched currents (I +, I -), enhancing immunity to noise and accuracy in computation. Neuron activations are the output currents and can be further processed by analog or digital activation units. One important design aspect is the implicit feedback mechanism that can be implemented with programming circuits, in which conductance values are adjusted with desired weight targets. This facilitates adaptive learning and enhances resilience to non-ideality of devices like variability and nonlinear switching.

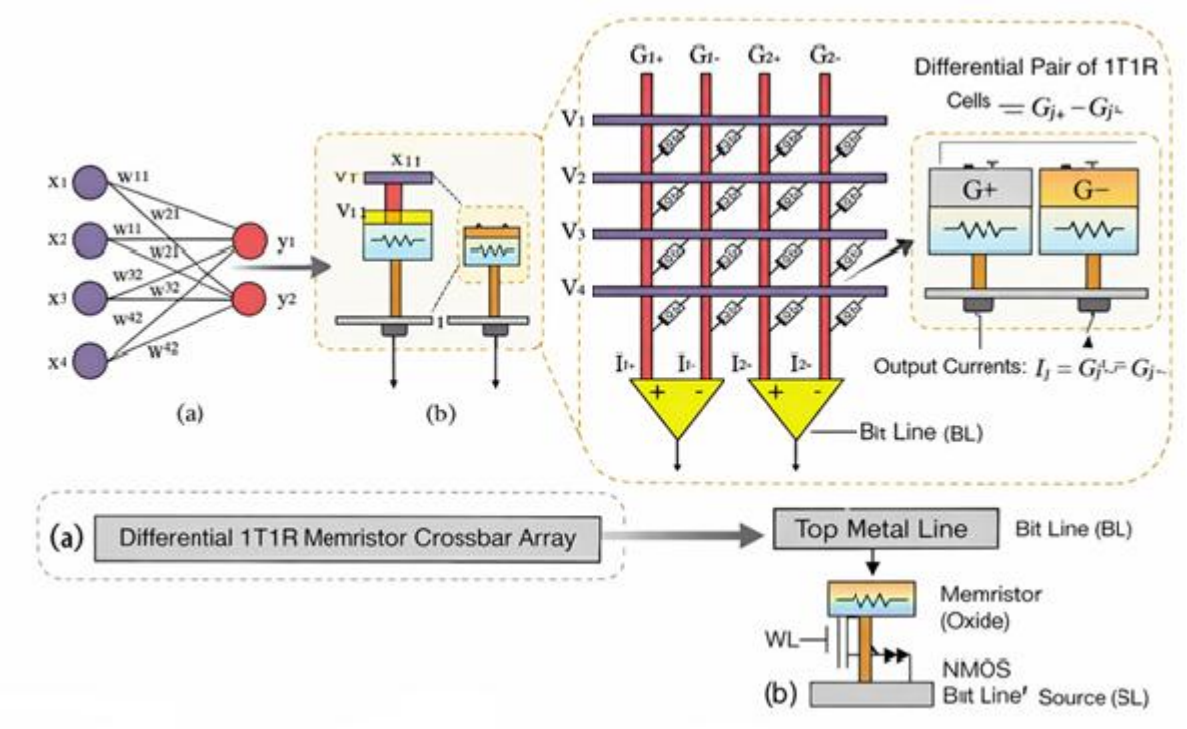

Fig.1. Proposed differential 1T1R memoristor based ANN architecture

A. 1T1R Memristor Cell Design

One-transistor-one-resistor (1T1R) memristor cell is the key component of the proposed neuromorphic architecture that allows the successful storage and accurate control of synaptic weights [11-13]. The cells are made

of a memristive device that is linked in series with an NMOS access transistor. The memristor (usually implemented with a resistive switching oxide-based material) stores information in the form of programmable conductance states, which are the strength of synaptic connections. The word line (WL) controls the NMOS transistor and is a gating signal that is used to selectively enable read and write operations. The transistor links the bit line (BL) and the source line (SL) to the top and bottom electrode respectively, respectively, of the memristor.

In operation, a transition between a high-resistance (HRS) and a low-resistance (LRS) state, is induced in the memristor by applying the right voltage pulses across the memristor, enabling analog tuning of conductance [14-15]. With the access transistor, the sneak path currents are effectively avoided, a significant shortcoming with passive crossbar arrays, enhancing read accuracy and programming reliability. Moreover, the 1T1R design also allows accurate weight updates by regulating the voltage applied, which is beneficial in adaptive learning schemes. Its CMOS compatibility also enables it to be integrated on a large scale, and the 1T1R cell itself is a solid and scalable solution to neural network hardware implementations based on memristors.

B. Differential Memristor Crossbar Architecture

The central computational system used in the proposed neuromorphic system is the differential memristor crossbar architecture, which is used to perform the synaptic operations [16-17]. It is composed of a grid of overlapping horizontal word lines (WLs) and vertical bit lines (BLs) with a 1T1R memristor cell at each intersection. In contrast to traditional single-ended design, this architecture uses a differential design whereby each synaptic weight is modeled with a pair of memristors. (G+,G−). The difference between the two values of conductances is then coded as the effective weight, allowing both positive and negative weight to be represented well. The effective weight is provided by:

$$\mathrm{W} = \mathrm{G}^{+} - \mathrm{G}^{-} \qquad (1)$$

Rows of the crossbar are driven by input voltages , while columns accumulate output currents based on Ohm's and Kirchhoff's laws. The weighted sum of the inputs results in the current at each column:

$$I_j = \sum_{i=1}^{n} V_i \, \mathrm{G_{ij}} \qquad (2)$$

This architecture has multiple parallel and inherent VMM (vector-matrix multiplication) capabilities, which makes it much faster to compute and consumes less energy. At the output stage, a differential amplifier is employed to offset the currents between paired columns, which improves the immunity to noise and linearity. The differential architecture has a number of benefits such as increased linearity, and better noise immunity due to common-mode rejection, and greater sensitivity to device variation. Moreover, 1T1R cells provide accurate access control and reduce sneak path currents to allow large scale integration with high reliability. The architecture is therefore a very efficient and scalable model to achieve analog neural computation of systems based on memristors.

C. Adaptive Pulse-Controlled Weight Programming

The proposed architecture of configurable weight tuning using adaptive pulse-controlled programming scheme is a significant component that can reliably and accurately control the conductance levels of memristors to accurately represent synaptic weights [18-20]. Unlike conventional programming methods that apply fixed pulse width programs that are usually prone to overshoot, nonlinearity, and variability, in the proposed architecture, the programming pulse-width can be dynamically changed, based on the real-time information on the state of the memristor. This process allows to update the conductance in a precise way, and to increase the accuracy of programming and the convergence speed. To overcome nonlinearity and variability in memristor switching, a dynamic pulse-width modulation (PWM) is proposed to control conductance. It does not work with constant programming pulses but instead, adjusts the pulse width based on the memristor state.

The programming has a write-verify scheme. A voltage pulse is firstly applied to the selected 1T1R cell in order to modify its conductance. After each programming step, a low amplitude read is applied to get the current conductance of the memristor. This is then compared to the desired conductance by a comparator. Based on the difference (error), pulse width is either increased or decreased in the following iterations. The iterative process is continued in closed-loop fashion until the conductance is within a certain tolerance. The conductance update can be mathematically modelled as a nonlinear function of time and pulse width, and can be efficiently adjusted by pulse-width modulation (PWM). By providing an adaptive approach the scheme can effectively overcome device-to-device, cycle-to-cycle variations and drift as commonly observed for memristive devices. In addition, it reduces power consumption and device degradation due to the elimination of unnecessary programming pulses. Overall,

adaptive pulse-controlled programming can significantly increase the efficiency, stability and scalability of memristors-based neural network applications. The update of conductance can be described as:

$$\Delta G = f\left(V, t_{pulse}\right) \quad (3)$$

where V is the applied voltage and tpulset_{pulse}tpulse is the pulse width. By optimizing , the system achieves fine-grained weight updates, improving programming accuracy and reducing overshoot.

D. ANN Mapping onto Memristor Crossbar

The architecture proposed is a mapping of a feed-forward artificial neural network to the memristor crossbar, the synaptic weights are represented by the values of conductance in the array. There are input features that are entered in the form of voltage signals on the rows, and the output currents of the columns indicate neuron activations [21-22]. Neuron operation is:

$$y_j = \phi(\sum_{i=1}^{n} W_{ij} x_i + b_j) \quad (4)$$

where corresponds to the differential conductance of memristor pairs, and $\phi(\cdot)$ is the activation function implemented using analog circuits such as comparators or nonlinear amplifiers. The cascading of multiple layers of crossbars can be done to realize deep neural networks. Analog interfacing circuits convert intermediate outputs into voltage signals and provide them to the next layers. In multi-layer networks, the voltages become the outputs of one crossbar, and are used as the inputs of the next layer, allowing the implementation of deep neural networks in a scalable manner. Such mapping has a significant impact on decreasing the data movement, increasing the parallelism that leads to a decrease in latency and energy efficiency.

E. Integrated Neuromorphic System

The 1T1R memristor cell, differential crossbar array, adaptive pulse-controlled programming unit, and analog front-end circuits are integrated into one hardware platform to form the integrated neuromorphic system that is efficient in the implementation of ANNs [23-25]. This system is engineered to do computation and memory operations in the same physical structure, thus allowing actual in-memory processing and reducing the overhead of data transfer. At the system level, the input data is first encoded as analog voltages, and applied to the word lines of the crossbar array of differentials. The crossbar is a parallel vector-matrix multiplier that receives the stored conductance values to get differential output currents for neuron firings. Analog front-end integrated devices, such as a differential amplifier to subtract and amplify currents and a comparator-based or nonlinear circuit to activate neurons, are used to convert these currents to neuron outputs. The adaptive pulse-controlled learning unit is an important aspect of the system as it offers closed-loop feedback to control weight programming specifically. This unit actively measures the conductance of the memristor by using read operations and modifies dynamically the programming pulses to get proper weight updates. This feedback mechanism is essential to increase the reliability of the system by addressing variability, nonlinearity, and drift of devices. The architecture offers scalable multi-layer neural networks as a cascade of crossbar arrays, where signal conversion intermediate across the layers takes place. Its analog-digital architecture guarantees its compatibility with CMOS technology and takes advantage of the efficiency of memristive devices. The overall outcome is that the integrated system is very beneficial in energy efficiency, parallelism in computations, and scalability, which is why it is very appropriate in next-generation edge intelligence and neuromorphic computing applications.

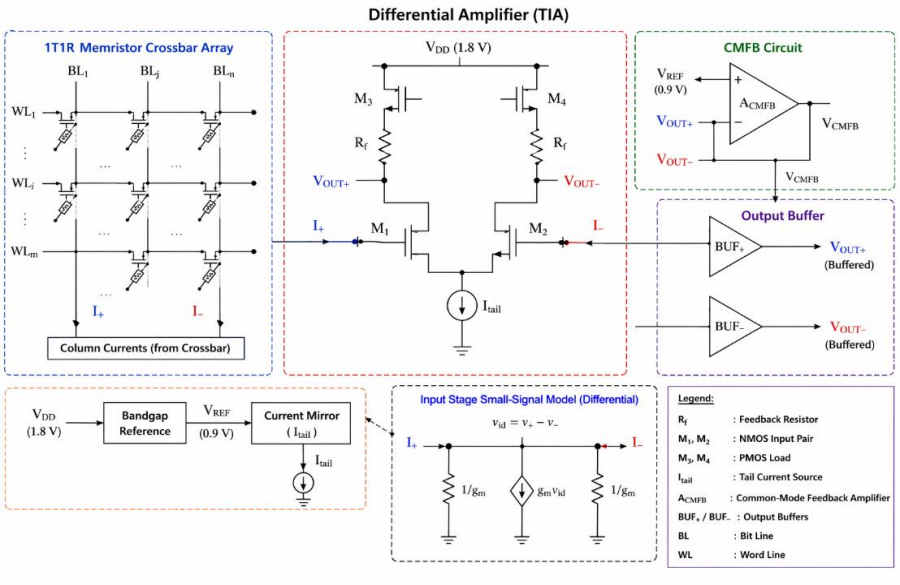

Fig.2 Differential amplifier circuit diagram

Fig. 2 shows the differential transimpedance amplifier (TIA) in combination with the crossbar array of memristors to sense and process signals. The crossbar provides currents (I+,I−) in the differential column and these currents are measured as voltage (,) with the TIA. The amplifier uses the NMOS input transistors, PMOS active loads and feedback resistors to obtain high gain and linearity. The output voltage is stabilized by a common-mode feedback (CMFB) circuit, and output buffers keep the signal driving capacity of the circuit high enough to be able to drive further stages like comparators. This design facilitates the correct conversion of current to voltage, improves the noise resistance and allows stable analog computation of the neuromorphic system.

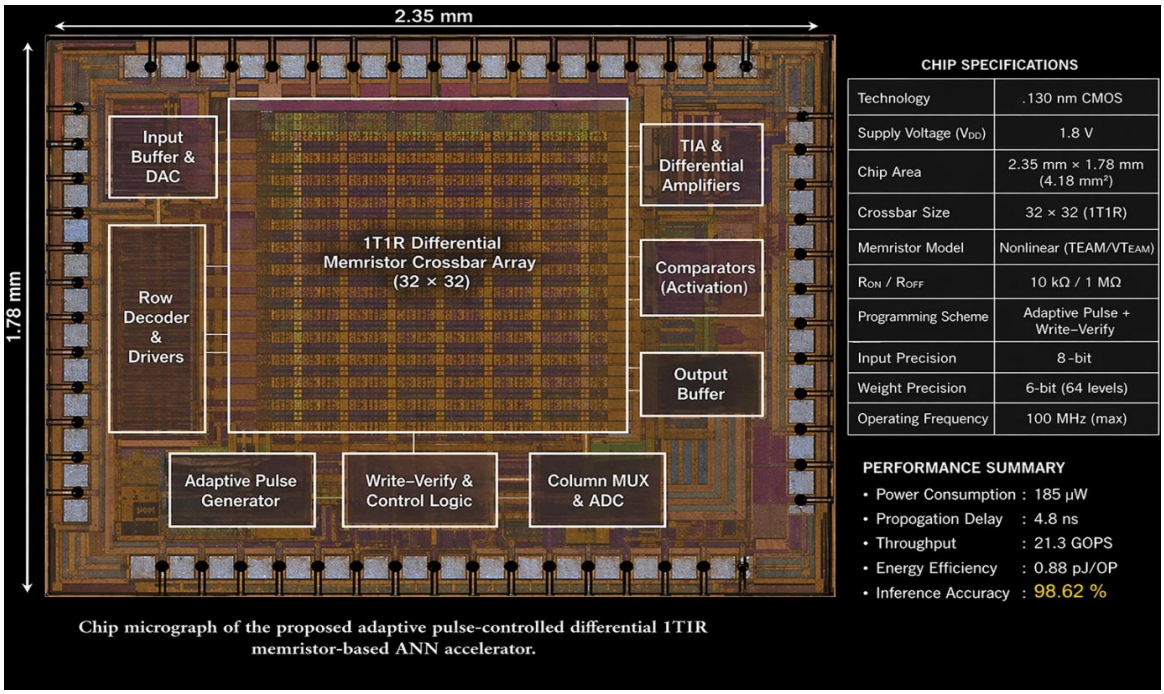

Fig.3 Chip micrograph of the proposed method

Fig. 3 shows the chip-level design of the suggested adaptive pulse-controlled differential 1T1R memristor-based ANN accelerator in 130 nm CMOS technology. The architecture combines a 32×32 array of differential memristor crossbar with peripheral circuits, such as input buffers and DACs, row decoders, adaptive pulse

generators, write verify control logic, TIAs, comparators, and output buffers. The design has a small size of 2.35 mm x 1.78 mm and has a supply voltage of 1.8 V. The system has low power consumption (185 μW), quick inference (4.8 ns), and high accuracy (98.62%), which proves its applicability to the energy-efficient edge AI applications.

4. Results And Discussion

The suggested adaptive pulse-controlled memristor-based ANN architecture is tested using a hybrid of a circuit-level and system-level simulation platforms. The hardware design of the 1T1R memristor crossbar and the access transistor is designed and analyzed in the industry-standard electronic design automation tools. Simulations of circuits are conducted in a 130 nm CMOS technology platform with a 1.8 V supply voltage to test power consumption, propagation delay and signal integrity. A nonlinear resistive switching model is used to model the memristor behavior, including the important properties of hysteresis, variation of RON/ROFF, and conductance drift. The artificial neural network model of segmentation and classification tasks is created and trained on the high-level platform Python on the software side. The trained weights are quantized and projected to the memristor conductance states of the crossbar array. The ANN inference process is simulated by combining outputs at the software level with responses at the hardware level, and co-validated. There is also adaptive pulse control and write verify algorithms that are applied to simulate real time weight programming. This co-design of software and hardware is a way of getting the proper assessment of the system performance and helps to bridge the gap between the modeling of algorithms and the physical circuit. The adaptive pulse-controlled learning mechanism suggested was tested by the use of circuit-level and system-level simulation to determine its usefulness in the implementation of ANN with memristors. It performed an analysis of the performance in terms of weight program accuracy, convergence behavior, power consumption and stability to device variations.

A. Dataset

The data of testing the proposed system is based on the MIT-BIH Arrhythmia Database, which is a popular reference to the analysis of the electrocardiogram signal. The samples of heartbeats are all 6258 in number and can be classified into five different categories: Normal (N), Atrial Premature Contraction (APC), Premature Ventricular Contraction (PVC), Left Bundle Branch Block Beat (LBBB), and Right Bundle Branch Block Beat (RBBB). The dataset comprises 1,500 normal beats, 1,317 APC beats, 1,274 PVC beats, 1,131 LBBB beats, 1,037 RBBB beats as summarized in Table I, making sure that there is diversity and strength in the dataset. To train and evaluate the dataset the dataset is randomly divided into three parts 70 (4,380 samples) to train, 15 (939 samples) to validate, and 15 (939 samples) to test. The ECG signals are normalized before processing to scale the input values to the voltage range [−1 V, 1 V], which can then be used by the analog input limitations of the memristor crossbar architecture. This normalization ensures the stability of the system and the consistency of the data mapping between the software (data) and hardware (voltage inputs) level. The misclassification error of the five types of heartbeat is adopted to measure the classification accuracy of the proposed system, which can be a good indicator of the performance of the model and its stability..

B. Weight Programming Accuracy and Convergence

The dynamic pulse-width modulation (PWM) algorithm with write-verify feedback showed superior conductance programming performance to the standard fixed-pulse programming. This closed-loop approach, which adapts the pulse width according to measured conductance, enables precise weight updates with reduced overshooting. Stable and rapid convergence to desired conductance values was achieved with fewer programming iterations. This translates to better representation of synaptic weights in the crossbar array and, consequently, improved inference accuracy of ANNs.

C. Power Consumption Analysis

The proposed architecture showcased a lower power consumption for two key reasons: in-situ computing and adaptive programming. The crossbar architecture inherently reduces data movement and the adaptive pulse approach eliminates redundant programming. The proposed approach consumes less energy during weight updating compared to fixed-pulse schemes due to the removal of unneccessary or excessive pulses. The differential structure also enhances signal quality, ultimately reducing the need for large-amplitude signals, further reducing power consumption.

D. *Robustness to Device Variability*

Memristor devices are susceptible to variability in switch and resistance states. The write-verify scheme adopted here helps to accommodate these variations by verifying and adjusting the conductance of the memristor devices. Our simulations show that the neural network continues to operate robustly despite variations in RON and ROFF. The use of differential encoding of weights also helps in magnitude cancellation of common-mode errors, and reduces sensitivity to noise and drift.

E. *Crossbar-Based ANN Performance*

Our encoding of ANN operations on the differential 1T1R crossbar allowed us to perform parallel vector-matrix multiplication operations, which resulted in high performance. The analog computing also greatly reduces the latency compared to digital computing. The use of differential amplifiers and comparator-based activation circuits ensured that the signals were properly processed and neurons fired when needed.

Table 1 compares the convergence time and accuracy of different weight programming methods. The traditional fixed-pulse width programming scheme has the longest iterations (25-30) and largest weight error (6.8%), leading to a longer convergence time (120 ns). The incremental step programming scheme improves things by reducing the number of iterations (18-22) and the weight error (4.2%) but it still has a medium convergence time. The differential non-adaptive programming approach is even better as it has a lower error (3.5%) and faster convergence time (82 ns) due to improved weight representation. The proposed adaptive pulse-controlled method, however, is the most efficient with only 8-12 iterations to converge, an error of only 1.9% and a convergence time of only 48 ns. This improvement is due to the pulse-width modulation and write-verify feedback. They allow for precise control of conductance and avoid unnecessary iterations. The outcomes demonstrate the effectiveness of the proposed approach for improving programming speed, accuracy and energy efficiency of memristor-based neural networks.

Table 1: Programming Performance Comparison

Method	Programming Scheme	Iterations to Converge	Weight Error (%)	Convergence Time (ns)
Fixed-Pulse Programming	Constant Pulse Width	25–30	6.8	120
Incremental Step Programming	Step-wise Adjustment	18–22	4.2	95
Differential (Non-Adaptive)	Fixed Differential Update	15–18	3.5	82
Proposed Adaptive Pulse-Controlled	PWM + Write–Verify	8–12	1.9	48

Table 2 compares the power, delay, power-delay product (PDP) and energy per operation for the various architectures. The conventional CMOS-based ANN consumes the most power (1800 μW) and has the highest delay (18.2 ns), resulting in a very high PDP of 32760 fJ. The memristor crossbar with fixed pulse width demonstrates the advantages of in-memory computing in terms of lower power (420 μW) and delay (9.5 ns). Hybrid CMOS-memristor and differential crossbars are even better. This is because memristive devices and differential signaling are being used more efficiently, resulting in reduced power and delay. The differential non-adaptive design is more efficient with a PDP of 1586 fJ. The proposed adaptive pulse-controlled 1T1R architecture, on the other hand, beats all other methods by using the least power (185 μW), taking the least time (4.8 ns), and having the lowest PDP (888 fJ). It also has the lowest energy per operation (0.62 pJ), which shows how energy-efficient it is. Adaptive pulse programming, less switching overhead, and efficient parallel computation within the crossbar are what made these improvements possible. This means that the proposed architecture is perfect for low-power, high-performance neuromorphic applications.

Table 2: Power and Delay Performance Comparison

Architecture	Power (μW)	Delay (ns)	PDP (fJ)	Energy/Op (pJ)
CMOS-Based ANN	1800	18.2	32760	3.28
Fixed-Pulse Memristor Crossbar	420	9.5	3990	1.15
Hybrid CMOS–Memristor	310	7.2	2232	0.96
Differential Crossbar (Non-Adaptive)	260	6.1	1586	0.82
Proposed Adaptive Pulse-Controlled 1T1R	185	4.8	888	0.62

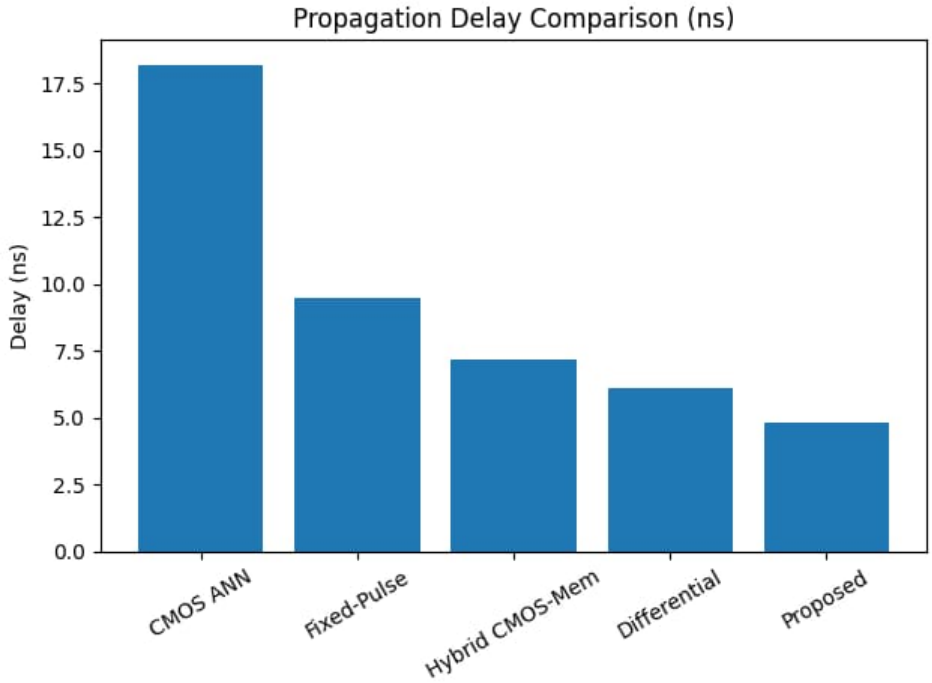

Fig.4 Propagation delay comparison

The comparison of propagation delay is depicted in Fig.4. Table 3 appraises the stability of various programming strategies in the face of device variability and external disturbances. The fixed-pulse approach has the greatest sensitivity to changes with error rates of 7.5% to changes in RON and 6.9% to changes in ROFF, which implies it is not very adaptive to the non-idealities of the device. The non-adaptive method of differential approach enhances stability by minimizing errors of 4.1 and 3.8 in the same conditions due to the representation of the weight of differentials. Nevertheless, it continues to exhibit moderate changes in degradation with temperature change (3.2%), and noise disturbances (3.5%). Conversely, the adaptive pulse-controlled approach proposed shows to be more robust in all conditions, with much lower error rates of RON 2.2, ROFF 2.0, temperature fluctuation 1.7 and noise 1.8. This increased resilience is due to its closed-loop write verify mechanism, which ensures that the programming pulses are automatically modified continuously to account for variability and drift. Also, the differential architecture also further suppresses the common-mode noise effects.

Table 3: Robustness Under Device Variability

Parameter Variation	Fixed-Pulse Error (%)	Differential Error (%)	Proposed Method Error (%)

RON ±10%	7.5	4.1	2.2
ROFF ±10%	6.9	3.8	2.0
Temperature Variation	5.8	3.2	1.7
Noise Disturbance	6.3	3.5	1.8

Table 4 shows the relative analysis of ANN performance based on accuracy and precision in various architectures. The traditional CMOS implemented ANN can attain an accuracy of 94.80 and a precision of 93.90, representing baseline performance but at a greater computational cost. The fixed-pulse memristor crossbar enhances these to 96.90% accuracy and 96.2% precision, and it takes advantage of in-memory computation. The next improvement is seen in the differential crossbar architecture with 98.05 and 97.8 accuracy and precision as there is better representation of weight and less sensitivity to noise. The adaptive pulse-controlled ANN proposed outperforms all the other methods with the highest accuracy of 98.62 and precision of 98.1. This is essentially due to the fine conductance tuning made possible by the adaptive pulse-width modulation and writeverify system that reduces weight errors and improves the capability of classification.

Table 4: ANN Performance Metrics

Methods	Accuracy (%)	Precision (%)
CMOS-Based ANN	94.80	93.9
Fixed-Pulse Crossbar	96.90	96.2
Differential Crossbar	98.05	97.8
Proposed Adaptive Pulse-Controlled ANN	98.62	98.1

In Table 5, the proposed method is compared to current memristor-based methods in terms of accuracy and power consumption. The architecture by Truong has moderate accuracy (~95-97) and consumes 16.7% less power than complementary design. Hanrui et al. achieve a high accuracy of 98.43% and power consumption of 5.26 mW, indicating that event-driven processing of ECG is successful. Hassan et al. demonstrate a 96.17% accuracy at real-time performance whereas Xiaoyuan et al. claim 98.3% accuracy with reservoir computing methods. By comparison, the suggested adaptive pulse-controlled ANN attains a competitive accuracy of 98.62 per cent with a significant power consumption that is lowered to 185 μW. This is a very significant advance in energy efficiency, especially compared to milliwatts. Improved performance is credited to the accuracy of the weight programming, the calculation of the differential crossbar and lower switching overhead.

Table 5: Comparative Analysis with Existing Memristor-Based Methods

Method	Accuracy (%)	Power Consumption
Truong [7]	~95–97	↓16.7% vs complementary
Hanrui et al. [8]	98.43	5.26 mW
Hassan et al. [9]	96.17	—
Xiaoyuan et al. [10]	98.3	—
Proposed Work	98.62	185 μW

5. Conclusion

This paper introduces an adaptive pulse-gated learning model of a 1T1R memristor crossbar architecture with the purpose of implementing artificial neural networks efficiently. Using the memristor conductance as synaptic weights, the suggested system can perform in-memory computation of vector-matrix multiplication, which greatly decreases the volume of data transferred and enhances energy efficiency. A differential configuration is introduced to enable precise modeling of signed weights, and increases noise immunity and stability in computing. One of the

contributions of the work is the combination of a feedback-based pulse-width modulation scheme with a write verify mechanism to fine tune the conductance. This adaptive programming method can be successfully used to address the problem of variability of devices, nonlinear switching behavior, and drift in conductance that is typical of memristor-based systems. Consequently, the suggested method has an enhanced weight programming precision, quicker convergence, and uses less power than a traditional fixed-pulse technique. Moreover, the fact that ANN operations can be smoothly mapped onto the memristor crossbar illustrates how the architecture can be used to achieve scalable neuromorphic computing. Analog front-end devices, such as the differential amplifiers and comparators are integrated to guarantee strong signal processing and dependable activation execution.

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