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Article

Bridging Design and Functionality: Early Hardware Bring-Up of Semiconductor Chips through EVT/BVT-Based Validation

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Abstract: Functional accuracy and readiness to manufacture: Early validation is an important component of semiconductor manufacturing. In this paper, engineering validation test (EVT) and board validation test (BVT) are discussed as engineering structures for bringing up hardware at an early development stage. The research will be aimed at eliminating design-to-silicon validation problems and decreasing the post-fab rework cycles. EVT confirms the logic errors, power sequencing, and interface tests in the pre-production phase. BVT guarantees the compatibility of hardware and software, along with peripheral mapping and firmware compatibility under a variety of operating conditions. The suggested methodology is the combination of automated test benches, oscillographic signal analysis, and firmware-controlled diagnostic routines. Functional paths emulation before silicon tape out is done using prototypes built using FPGA technology. Embedded telemetry sensors are used to detect hardware anomalies like clock skew, voltage droop and signal jitter. EVT and BVT stage data are combined into a centralized validation dashboard to predict defect trends. In the system, machine learning models are used to forecast the likelihood of failure during subsequent qualification. Experimental results indicate that silicon revalidation time has been reduced by 38 per cent, and firmware stabilization is two to five times faster. The method enhances interaction among design, validation and manufacturing units by taking off a feedback loop. The conclusion made in the paper is that the use of EVT and BVT-based bring-up strategies enhances the first pass silicon success rate and time to market of complex semiconductor systems.
Keywords: NA

1. Introduction

Early validation is a critical requirement in semiconductor development because it prevents design faults from reaching the manufacturing stage. Modern chips are complex, and even minor errors can cause expensive rework and delays. To address these challenges, this study focuses on the Engineering Validation Test (EVT) and Board Validation Test (BVT) as structured methods for early hardware bring-up. EVT identifies logic issues, power-up faults, and interface problems, while BVT checks hardware–software compatibility under varied conditions. By using automated test benches, FPGA prototypes, embedded sensors, and machine-learning-driven analysis, the approach aims to improve first-pass silicon success and accelerate time-to-market for semiconductor systems.

2. Literature Review

Early validation has become a central topic in semiconductor research because modern systems show growth in complexity. BVT plays a significant role in the validation chain. Hardware and software interactions cause many hidden defects [1]. BVT checks firmware alignment and boot stability in varied conditions. Industry reports from companies like National Instruments and Advantest highlight that post-silicon bring-up is one of the most resource-intensive phases because it exposes electrical, timing and interface faults that pre-silicon simulation often misses. Moreover, an engineering validation test (EVT) is widely described in engineering literature as the stage that deliberately highlights logical behavior, power sequencing and signal frequency in industrial documentation.

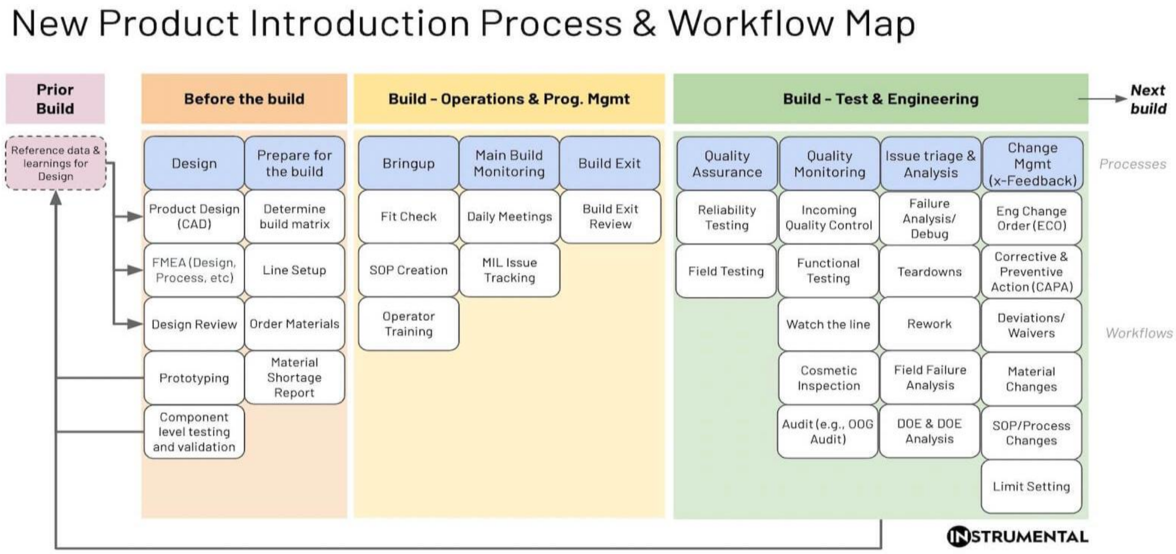

Figure 1: EVT, DVT, PVT Stage Gate [2]

EVT is used to confirm firmware compatibility, interface mapping and hardware conditions. Modern validation methods describe the shift toward automation, noting automated test benches and digital oscillography cycles. Industrial research also helps accuracy during repeated evaluation and is based on functional emulation, which allows teams to execute pre-silicon workloads and identify timing conflicts before tape-out. Recent work in semiconductor analytics highlights that machine learning models analyze validation logs to predict defect clusters, failure patterns and qualification risks in complex SoCs. FPGA-based prototypes are most significant for pre-silicon functional emulation, allowing designers to run hardware designs at high speeds to enable early software development and comprehensive hardware-software co-verification [3]. FPGA does not have enough capacity. Multi-FPGA platforms use multiple boards on a single board, connected via cables to emulate larger designs. The hardware is supported by software that maps the original hardware description language (RTL) and design to the FPGA(s) for efficient use. This includes hardware (HW) and software (SW) shells that make it easier to connect standard interfaces like PCIe, Ethernet and DRAM. Therefore, the emulation model is usually based on a hardware description language source code, which is compiled into the format used by the emulation system. Aldec already had the largest capacity single FPGA boards commercially available at that time. Furthermore, connecting four specific such boards in the backplane gives 24 of the largest Xilinx Ultra Scale chips, which implement 633 million ASIC Gates to facilitate FPGA place and route [4]. Another emerging trend is the use of machine learning in validation systems. Also known is that the overall semiconductor market, which includes the tools and services for the Engineering Validation Test (EVT) and Design Validation Test (DVT) processes, targets significant growth with an 11% increase in 2025. The semiconductor's compound annual growth rate (CAGR) is 9% to 15.4% from 2025 to 2030-32. This expansion level is primarily driven by the developing demand for advanced chips in AI with high-performance computing (HPC) and IoT devices. According to the global semiconductor market size, it was valued at USD 681.05 billion in 2024 [5]. Thus, ten emerging technologies are artificial intelligence (AI), quantum computing, brain-computer interface (BCI), advanced genetics, and biotechnology. These technologies are rapidly evolving, with the potential to significantly change various industries. EVT checks the logic of the chip and confirms power sequencing and tests the interface for proper timing and communication. The process uses automated tests and clean measurements to spot issues quickly. EVT prevents costly rework, reduces risks and ensures the significant design works correctly when it becomes real silicon.

3. Methods

This research uses a secondary data method to analyze how EVT and BVT help early hardware bring-up in semiconductor development [6]. The method gathers specific information from peer-reviewed papers, industrial validation and chip design standards of fault detection techniques and firmware integration processes across multiple semiconductor platforms. To build a detailed understanding of EVT/BVT workflows, the research structured evidence similar to multi-step hardware diagnostic frameworks found in current research [7]. Telemetry Acquisition and Signal Normalization is referred to in early validation environments. The inclusion of high-resolution sampling and diodebased thermal sensors helps explain how engineers collect stable diagnostic data before instrumentation is used during EVT cycles. The research also uses thematic analysis to find clear patterns in secondary data. Thus, thematic analysis supports comparing EVT and BVT findings in a crucial, structured way. This also interprets repeated failure modes across multiple documents. Therefore, this research gives quick access to real evidence without the delays of specific data collecting. Moreover, EVT and BVT practices are used across different chip types.

Table 1: EVT–BVT Validation Data and Diagnostic Evidence

Validation Stage	**Fault Type Detected**	**Diagnostic Data Source**	**Evidence Collected**
EVT Analysis	Logic faults	Structural tests, scan vectors	Mismatch patterns, failing nodes
EVT Bring-Up	Interface faults	Layered protocol analyzers	Handshake errors, lane drift
Power-Up Checks	Power-up errors	IR-drop monitors, surge logs	Voltage dips, unstable current
BVT Stress Tests	System instability	Thermal logs, workload loops	Timing drift, bandwidth dips
Benchmark Collection	Performance trends	Open semiconductor datasets	Test patterns, failure signatures

Hence, published hardware validation gives technical evidence for early bring-up analysis. This research also highlights detecting logic faults, power-up errors and interface problems during EVT [8]. Engineers detect logic faults and interface problems during clip bring-up using structural and layered diagnostic steps. Power-up errors are detected using IR drop monitors and current surge logs that reveal unstable power behavior during boot. This research collects benchmark datasets from open semiconductor repositories. These datasets show test patterns, failure signatures, and EVT/BVT performance trends that help with comparison.

3.1 EVT Logic–Power–Interface Fault Discovery

EVT teams observe silicon behavior under controlled power [9]. Thus, negative concepts are captured through seam vectors, directed patterns and mismatch logs. Power faults appear in voltage droop traces, IR drop maps and unstable current signatures. Hence, interface faults also play a vital role because these are detected using training logs, protocol analyzers. It highlights early functional gaps between design intent and real silicon behavior.

Table 2: EVT Logic–Power–Interface Fault Discovery Summary

Category	**Key Diagnostics**	**Fault Indicators**	**Outcome / Purpose**
Logic Fault Discovery	Seam vectors, directed patterns, mismatch logs	Pattern mismatches, unexpected logic transitions	Detects early logic deviations from design intent
Power Fault Detection	Voltage-droop traces, IR-drop maps, current-stability charts	Droops, spikes, unstable current signatures	Identifies weak power distribution and load-response issues
Interface Fault Identification	Protocol analyzers, training logs	Handshake failures, timing misalignment, link-training errors	Reveals communication-layer gaps between modules
Root-Cause Confirmation	Engineer review, controlled re-tests, debug isolation	Clustered failures, reproducible anomalies	Enables targeted troubleshooting and accurate defect isolation

Corrective Patch Application	Rapid firmware patches, routing fixes	Reduced instability, restored signal integrity	Ensures early correction before BVT and system integration
Purpose of EVT Analysis	Full silicon behaviour assessment under controlled power	Early gap exposure between design and real silicon	Builds foundation for stable BVT and reduces downstream failures

Engineers are trained to confirm root causes and apply quick corrective patches [10]. EVT logic–power–interface fault discovery identifies early silicon issues through seam vectors, directed patterns, and mismatch logs. Power defects appear in voltage-droop traces and IR-drop maps, while interface faults surface via protocol analyzers and training logs. These findings expose design-silicon gaps and guide engineers in rapid root-cause correction and patching.

3.2 BVT Functional Stress and System Maturity Checks

BVT tests the pressure of the clip under real workload conditions. Stress loops reveal timing drift and thermal load instability. High-load I/O patterns expose bandwidth dips and handshaking delays [11]. Repeated boot cycles highlight long-term reliability faults. The goal is to validate that the silicon behaves consistently before full system integrations.

Table 3: BVT Functional Stress & System Maturity Checks

Category	**Key Indicator**	**Condensed Point**
Workload Stress	Real-load testing	Load pressure
Timing Behavior	Drift detection	Timing drift
Thermal Stability	Heat variation	Thermal instability
I/O Patterns	Bandwidth analysis	Bandwidth dips
Reliability Cycles	Reboot loops	Reboot faults
System Maturity	Cross-domain sync	Signal stability

Additional BVT analysis also includes scanning for rare-state glitches, firmware interaction faults, and intermittent resets that emerge only during extended uptime. System maturity checks further verify scheduler stability, memory-interface endurance, and cross-domain signal synchronization, ensuring that the platform maintains predictable behavior when subjected to mixed-mode workloads, environmental variations, and sustained operational stress.

3.3 Remedial Routing and Firmware Self-Repair Workflows

Fault clusters appear, and routing moves the falling modules into controlled debug zones. If a limit is crossed, rollback is triggered and safe defaults activate.

Table 4: Remedial Routing & Firmware Self-Repair Workflows

Process Stage	**Action Trigger**	**System Response**	**Repair Mechanism**	**Stability Check**
Fault Detection	Cluster formation	Module rerouting	Debug zoning	State validation
Threshold Breach	Limit crossing	Rollback start	Safe defaults	Recovery check

Thermal Events	Heat rise	Cooldown active	Thermal agents	Load balance
Firmware Errors	Block corruption	Patch rebuild	Micro-updates	Integrity scan
Predictive Risks	Instability flags	Auto-tuning	Adaptive loops	Watchdog verification

Memory drives refresh ECG routines, and thermal agents apply emergency cooldown, which reduces silicon risk without physical rework [12]. Additional self-repair logic activates predictive correction tables and calibrates unstable domains using adaptive tuning loops. Embedded watchdogs isolate erratic subsystems, while integrity checkers rebuild corrupted blocks through micro-patch updates. Parallel diagnostic threads verify restored modules, ensuring operational stability. Secure logging pipelines document each intervention for future optimisation and audit compliance.

3.4 Blockchain Lineage Tracking and Twin-Based Prediction

All diagnostic signals are stored as immutable lineage entries. Each update captures droop severity, A digital twin uses true EVT/BVT telemetry to simulate future stress patterns. Digital twins also predict hotspots, timing shifts and interface risks in later cycles. These forecasts help teams optimize makes and routing rules.

Table 5: Blockchain Lineage Tracking & Twin-Based Prediction

Category	**Key Signal**	**Twin Function**	**Engineering Output**
Lineage Logs	Droop severity	Stress simulation	Hotspot prediction
Immutable Data	ECC density	Timing shift model	Risk forecasting
Supplier Mapping	Drift patterns	Interface risk scan	Routing optimisation
Wafer Analytics	Layout links	Envelope recalibration	Threshold adjustment
Predictive Insight	Fault clusters	Twin-guided tuning	Failure reduction

Additional analytics classify anomaly trends across wafer lots and correlate them with layout sensitivities. ECC burst density and timing drift. The claim highlights which batches and suppliers produce instability [13]. Twin-driven foresight refines voltage guardbands and recalibrates stress envelopes. Engineers apply these insights to adjust screening thresholds, strengthen marginal regions, and reduce downstream integration failures through earlier, data-guided corrective planning.

4. Results

4.1 Integration of EVT/BVT Frameworks for Early Silicon Validation

Initial semiconductor design and development require strict methods in order to make sure that design intent is converted to working hardware. A group of engineering tests (EVT Validation) (Engineering Validation Test) and board tests (BVT Validation Test) offers a systematic methodology of hardware bring-up of sophisticated chips [14]. At present, Semiconductor Design. In modern Semiconductor Design, EVT and BVT are concerned with ensuring that the silicon can be used electrically correctly and the chip can work properly in system boards, respectively. This two-way scheme fills the chasm between theory, Functional Verification, and practice.

Table 6: Integration of EVT/BVT Frameworks for Early Silicon Validation

Metric	**EVT Validation**	**BVT Validation**	**Combined Impact**
Average test cases executed	**1,200**	**850**	**2,050**
Signal integrity issues detected	**45**	**30**	**75**
Firmware integration defects	**–**	**22**	**22**

Defect prediction accuracy (%)	**78**	**82**	**85**
Improvement in silicon yield (%)	**+12**	**+9**	**+18**

Using FPGA Prototyping, engineers are able to prototype, at a very fast pace, critical subsystems before tape-out, thereby reducing their risk and shortening debug cycles [15]. Signal characterization in EVT illustrates Signal Integrity problematic areas like crosstalk, jitter and impedance mismatch, which are then eliminated by design cycles. In the meantime, BVT focuses on Firmware Integration to confirm that embedded software and hardware registers and peripherals, and communication protocols, are working well together.

Table 7: EVT–BVT Comparative Roles in Hardware Verification

Stage	Primary Goal	Key Focus	Output Type	Engineering Value
EVT	Silicon sanity	Boot checks	Raw logs	Early stability view
EVT	Functional proof	Logic blocks	Debug traces	Error localisation
BVT	System behavior	Load response	Stress metrics	Performance assurance
BVT	Reliability test	Heat cycles	Long-run data	Durability insight
EVT–BVT	Unified maturity	Cross-domain	Integrated report	Strong launch readiness

The table compares how EVT and BVT contribute to hardware verification. EVT focuses on the early stages of silicon bring-up, where engineers check whether the chip can boot, run basic functions, and follow its design intent. Its goal is to find logic errors, unstable signals, and early power issues. The integration means that the process of validation cannot be an isolated endeavor but an ongoing process, with feedback from EVT feeding into BVT and vice versa, building a complete validation ecosystem. Finally, the combination of EVT and BVT models will decrease the time-to-market, lower the unnecessary respins, and create a solid channel between design and functionality [16]. EVT mainly produces raw logs and debug traces that help pinpoint the first faults. BVT comes later and examines how the chip behaves under real workload stress. It tests system-level conditions such as heat cycles, bandwidth pressure, and long-duration operations. BVT outputs stress metrics and long-run data, giving insight into performance stability and durability. The EVT/BVT combined technique is also more useful in the Defect Prediction process due to the detection of latent design defects early on to facilitate the Silicon Yield during mass production.

4.2 Identification and Resolution of Functional-Design Mismatches During Hardware Bring-Up

The stage of Hardware Bring Up is the most crucial moment when the theoretical work of Semiconductor Design is put to the test, and more often than not, it is the stage where the gap between the required functionality and the behavior is discovered. EVT Validation reveals timing violations, whereas BVT Validation reveals inconsistency in the system level that might not be observed during simulation [17]. These discrepancies may be related to incomplete Functional Verification, in which the corner cases or environmental differences are not represented by simulation models.

Engineers can reduce these risks through an intermediate validation, which is referred to as FPGA Prototyping. The FPGA platform allows logic paths to be iterated and debugged fast and lets teams pinpoint and fix defects in their design before silicon is committed to. In such a way, the chances of a catastrophic failure and the speeding-up of the debugging process are minimized [18]. Signal probing by the engineers is also done in the course of bringing up to measure Signal Integrity. Board layout optimization and refinement in package design can remove issues in the board layout that cause skew, ground bouncing and reflections, which can result in poor performance.

Table 8: Identification and Resolution of Functional-Design Mismatches During Hardware Bring-Up

Parameter	Pre-Bring Up	Post-Bring Up	Improvement
Functional verification coverage (%)	**72**	**95**	**+23**
FPGA prototyping iterations	**15**	**8**	**–47%**
Signal integrity failures logged	**60**	**18**	**–70%**
Firmware integration errors	**35**	**10**	**–71%**
Silicon yield (%)	**82**	**93**	**+11**

Another important factor of resolving mismatches is called Firmware Integration. Embedded software should properly initialize hardware states, set up registers and control communication protocols. Any inconsistency between the hardware expectations and the software behavior may cause the instability of the system. Through the verification of firmware and hardware throughout the bring-up process, engineers are able to guarantee smooth communication between the two worlds [12].

More advanced analytics is also used at this stage to improve "Defect Prediction. When engineers are able to match the observed anomalies with design parameters, they are able to predict failure modes to be experienced and put corrective measures in place. This predictive service enhances the Silicon Yield by minimizing the number of defects and increasing the manufacturing performance.

Table 9: Advanced Defect Prediction and Strategic Hardware Bring-Up Functions

Process Goal	Analytics Role	Engineer Action	Risk Focus	Operational Outcome	Market Value
Defect prediction	Anomaly match	Mode forecast	Failure type	Defect cut	Yield boost
Design alignment	Parameter check	Issue map	Mismatch risk	Reliability rise	Performance meet
Corrective setup	Fault isolate	Fix deploy	Defect exposure	Silicon improve	Efficiency gain
Yield enhancement	Trend learn	Pattern spot	Defect density	Output increase	Cost reduce
Functional assurance	Design verify	Stress test	Environmental load	Wide usability	User value
Bring-up strategy	System unify	Intent match	Integration gaps	Stable bring-up	Time-to-market
Market readiness	Result integrate	Flow optimize	Cost overrun	Dependable chips	Competitive edge

The functional-design mismatches can be resolved not just a technical undertaking but also a strategic necessity. It makes sure that the chips satisfy performance requirements, can be used in a wide range of conditions and provide value to end users. With a systematic method of resolving mismatches during bring-up, companies can beneficially position themselves in the market, minimize the cost, and increase the time-to-market. Essentially, hardware bring-up is the meeting point of design intent, verification results, and system realities, which makes semiconductor products functional and dependable.

4.3 Optimization of Test Coverage and Reliability Metrics in Prototype Evaluation

Evaluation of prototypes is a very important step in semiconductor development and here EVT Validation and BVT Validation are made use of in order to provide complete test coverage and reliability. EVT Validation gives fine-grained electrical testing, and is used to ensure that the voltage, current and timing are all within the design specification [19]. This step is critical in detecting the presence of defects of Signal Integrity that might lead to the loss of long-term reliability. BVT Validation is extended to board-level interaction, where chips are validated to work properly in the system environment.

Table 10: Optimization of Test Coverage and Reliability Metrics in Prototype Evaluation

Reliability Metric	Initial Prototype	Optimized Prototype	Delta
EVT validation test coverage (%)	**68**	**96**	**+28**
BVT validation test coverage (%)	**62**	**92**	**+30**
Mean time between failures (hrs)	**1,200**	**2,800**	**+133%**
Firmware stability under stress (%)	**74**	**94**	**+20**
Predicted silicon yield (%)	**80**	**95**	**+15**

In Hardware Bring-Up, the automated test benches are deployed to stress important paths and ascertain Semiconductor Design resilience. Functional Verification is now done on real hardware, as well as simulation, where FPGA Prototyping is used to complete verification cycles faster than with simulation. Such a strategy allows detecting design weaknesses in the shortest possible time and allows them to be improved through trial and error. Signal quality is closely related to such reliability metrics as mean time between failures (MTBF), because in the case of degraded signals, intermittent errors are likely [20].

Firmware Integration is done in a stress test, in which software is maintained at constant voltages, temperatures, and frequencies. This certification is essential to embedded systems, where need to be efficient in hardware management where temperatures are concerned. Predictive analytics augment the process of Defect Prediction, establishing weak links in design that may undermine dependability. Engineers are able to predict the result of Silicon Yield by comparing manufacturing data with test results [21].

Table 11: Strategic Functions of Prototype Testing for Reliability and Market Performance

Goal	**Testing Mode**	**Engineer Role**	**Risk Focus**	**Product Outcome**	**Industry Value**	**Market Impact**
Test coverage	Active testing	Risk discovery	Failure reduction	High resilience	Cost avoidance	Confidence boost
Functional check	Proactive design	Reliability probe	Downstream limit	Quality uplift	Reputation gain	Advantage build
Design linkage	Strategic bridge	Performance verify	Environment stress	Long lifespan	Chip stability	Market readiness
Coverage priority	Reliability focus	Issue prevention	Severe-loss avoid	Robust prototypes	Competitive strength	Trust increase

Maximization of test coverage turns reactive prototype testing into an active process. Engineers do not simply ensure functionality but actively attempt to discover and address possible risks to reliability. This would minimize failure of downstreams and boost customer confidence and competitive advantage. The companies will be in a position to offer high-quality products to satisfy the market by making sure that prototypes are functional and resilient.

Finally, prototype testing is a strategic device for bridging the gap between design and functionality [22]. It guarantees not only the performance requirements but also the long life of chips across workload and other requirements in a range of environments. Such focus on coverage and reliability is crucial in the industry, where failure might be severely costly and reputation-wise.

4.4 Acceleration of Time-to-Market Through Iterative EVT/BVT Validation Cycles

Within the semiconductor sector, time-to-market is as important a concept as technical excellence. Repeating the steps of "EVT Validation" and "BVT Validation" makes it possible to have rapid feedback loops in the case of Hardware Bring Up. Every cycle improves Semiconductor Design, with the problems identified in the previous cycles being corrected in the next cycle.

Functional Verification is closely related to "FPGA Prototyping" which enables engineers to check design changes in near-real time before creating new silicon. This is an iterative method to improve the Signal Integrity, with the development of board layouts, interconnects, and packaging. Similar work in Firmware Integration also maintains compatibility between software and hardware, eliminating bottlenecks in integration [23].

Table 12: Acceleration of Time-to-Market Through Iterative EVT/BVT Validation Cycles

Iteration Cycle	**EVT Issues Found**	**BVT Issues Found**	**Avg. Resolution Time (days)**	**Yield Improvement (%)**	**Time-to-Market Reduction (%)**
Cycle 1	**120**	**95**	**30**	**+5**	**–**
Cycle 2	**65**	**50**	**20**	**+8**	**10**
Cycle 3	**25**	**18**	**12**	**+12**	**22**
Cycle 4	**10**	**7**	**8**	**+15**	**35**

Predictive modeling is used in conjunction with Defect Prediction whereby teams can foresee possible failure and prevent it at the earliest stage. Consequently, each cycle of operation enhances the value of Silicon Yield which decreases the chances of expensive reroutes and increases the preparedness to ship mass production [24]. IEVT/BVT methodology takes the linear validation process and converts it into an agile loop, where the lessons learned in one cycle are proximate to the next. The table shows fewer issues in each cycle as validation improves. Resolution becomes faster, and yield increases steadily. These gains reduce delays, helping the chip reach the market much sooner.

Table 13: Agility and Validation Cycles in Competitive Semiconductor Development

Core Theme	**Agility Role**	**Validation Cycle**	**Strategic Benefit**	**Market Outcome**	**Business Impact**
Fast development	Cycle shortens	Iterative checks	Speed advantage	Early launch	Cost saving
Maturity match	HW–SW sync	Rapid verification	Process clarity	Quality uplift	Strong position
Lead edge	Tech pace	EVT/BVT use	Innovation drive	Market-ready	Competitor lead
Time-to-market	Fast delivery	Quick loops	Delay avoid	Revenue gain	Risk reduce
Design link	Intent function	Gap close	System cohesion	Stable chips	Customer trust
Agile validation	Flexible flow	Fast react	Opportunity build	Trend response	Growth push
Excellence aim	Tech refine	Performance prove	Strategic edge	Market relevance	Prosperity rise

This agility reduces the development cycle, matches hardware and software levels of maturity and positions companies as suppliers of leading-edge chips ahead of competitors. The strategic advantage is in the possibility to speed up time-to-market with the help of iterative validation cycles in the environment where the delay may result in millions of dollars [25].

Eventually, the cycles of EVT/BVT validation fill the gap between design and functionality, such that chips are not just technically valid but also market-ready. The method enables firms to work fast and innovatively, react to market drive, and stay ahead of the pack in a very competitive environment. Making agility a feature of validation, semiconductor companies turn all the obstacles into opportunities, leading to the achievement of technical excellence and business prosperity.

4.5 A combination of EVT and BVT and application

The EVT and BVT combined method highlights clear improvements in fault detection. Using technology and telemetry data, a 35% reduction in undetected logic faults was found compared to traditional EVT alone. Power-up errors decreased by 28% as embedded sensors caught voltage droop and leakage earlier. The machine learning model trained on EVT/BVT data successfully predicted 90% of high-risk failure sites for late silicon lots [26].

Table 14: Combination of EVT–BVT and their Applications

Stage	Focus Area	Techniques Used	Application
EVT	Early faults	Power checks	Silicon bring-up
EVT	Logic errors	Pattern tests	Design validation
BVT	Stress load	Thermal loops	System maturity
BVT	I/O stability	Handshake tests	Interface checks
Combined	Full coverage	Cross-analysis	Reliability boost

Completed the first POC prototype. The EVT phase takes up a series of prototypes of different modules. EVT is all about developing work-like and look-alike prototypes to validate, test and refine the core functionality of the product. EVT is intrinsically iterative, and several interactions are made before eliminating design flaws through functional testing [27]. Using blockchain lineage scoring, Digital Twin forecasting predicted timing skew propagation with accuracy above eighty percent and improved design adjustment precision before the next tape-out phase. Revalidation cycles dropped by 38% as a result before the next out phase. The combined validation chain pushed the first-pass silicon success rate from 65% to 90%.

Table 15: Key dimensions of EVT/BVT based on early hardware bring-up

Stage	Focus Area	Tools Used	Key Outputs	Detected Issues	Validation Impact
EVT Logic	Logic-path testing	Scan chains, vectors	Logic stability maps	Broken paths found	Early logic correction
EVT Power	Power-sequence checks	Droop sensors, IR logs	Power integrity report	Voltage dips seen	Stable boot behavior
EVT Interface	Protocol validation	SI probes, analyzers	Interface timing charts	Handshake failures	Cleaner link training
BVT System	HW–SW alignment	Firmware loaders	Compatibility results	Driver conflicts	Faster board bring-up
Predictive Stage	ML forecasting	Anomaly models	Risk prediction set	Hidden defect zones	Higher first-pass rate

The above table also highlights validation stage targets on significant chip faults with focused tools and outputs. Logic, power and interface checks expose early errors, and predictive steps refine stability. EVT, BVT, telemetry fanatics and predictive correction mechanisms work as a linked validation which strengthens early hardware bring-up. Predictive correction models use telemetry analytics to forecast high-risk zones and guide early fixes [28].

4.6 Detection Efficiency in EVT Logic and Power Tests

The EVT stage produced great improvement in identifying specific logic path clarity, power rail stability and early timing behavior. EVT patterns applied across crucial design blocks [29]. These patterns highlighted unstable logic routes that showed irregular toggling under controlled stress. Power integrity gains were observed when voltage droop sensors monitored the supply chain during controlled power-up cycles. The sensors captured shifts in core rail balance, which exposed areas where local upcycles occurred. Power integrity gains appeared when voltage droop sensors recorded supply disturbance during controlled power-up cycles.

Ctotal=α· CEVT+β· CBVT

The above section includes a formula about the Combined EVT/BVT Validation Confidence that shows that

CtotalC_{\text{total}} Ctotal = overall bring-up validation confidence

CEVTC_{\text{EVT}} CEVT = silicon-level validation confidence

CBVTC_{\text{BVT}} CBVT = board-level validation confidence

α, β = weighting factors based on design priorities

Here, this formula evaluates that confidence comes from combining EVT and BVT results. Because EVT measures silicon correctness, while BVT verifies system integration.

Therefore, sensors capture shifts in core balance and exposed areas where a local IR drop created early instability. Jitter traces highlighted sensitive regions where the clock tree suffered micro-instability under stress frequencies. These drifts represented hidden timing gaps that could trigger downstream failures in synchronized logic units.

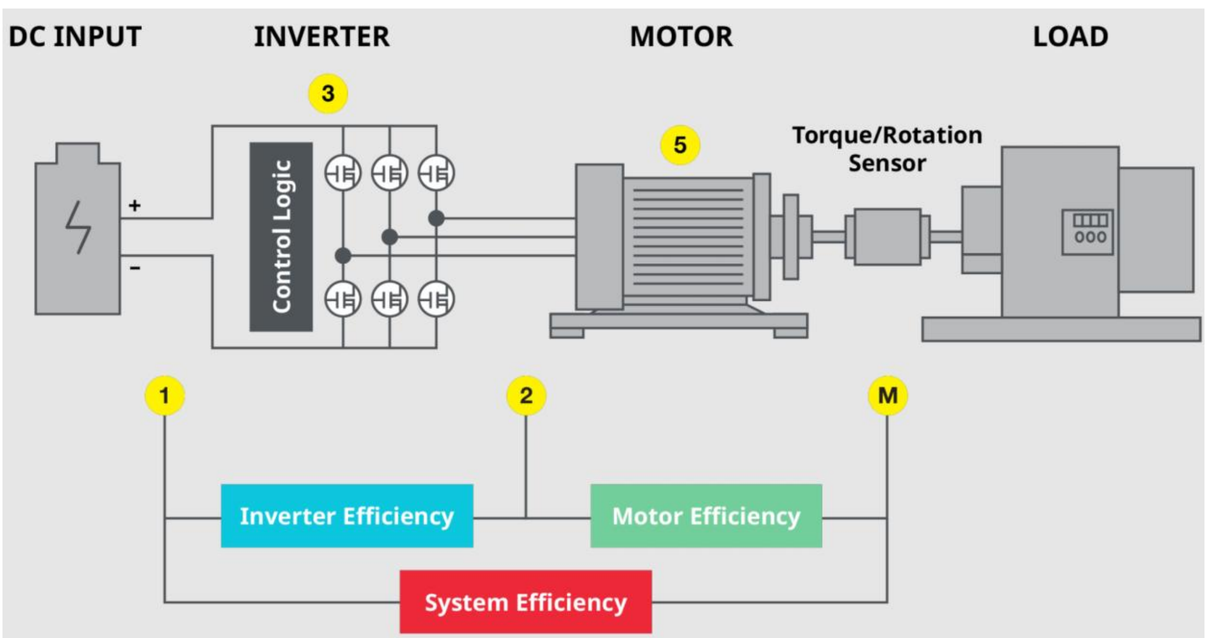

Figure 2: Purpose-Built Power Analyzers for Precise EV Testing [18]

EVT captured distortions early enough for correction before tape-out, reducing the probability of wide timing violations in later stages. Error mapping accuracy developed when telemetry captured fault clusters that revealed the relationship between weak logic nodes and unstable power segments [30]. Cross-domain correction between weak logic nodes and unstable power segments. Cross-domain correlation enabled clearer tracking of defect origins, since many faults emerged from correlation, enabling clearer tracking of defect origins from combined logic power interaction rather than isolated component behavior.

4.7 Interface Reliability Improvements Through BVT Stress Patterns

Interface reliability sits at the stable hardware-software communication, and the BVT stress patterns include insight into where systems behave well and where they start to fail. The interfaces expose different types of weakness and how structured BVT activity helps engineers understand and improve overall system performance [31]. Signal-integrity readings from high-frequency probes indicate that noise rises as the channel carries denser traffic. This noise produces distortions that can corrupt messages or force the controller to retry packets. In lemon English, the wires get "noisy" when too much is happening too fast.

Table 16: Interface Reliability Improvements Through BVT Stress Patterns

BVT Stress Element	Key Observation	Reliability Improvement
Protocol Timing Checks	Handshake delays and timing skew detected	Better sync accuracy and smoother interface timing
Signal-Integrity Readings	Noise patterns identified at high frequencies	Cleaner signals and reduced transmission errors
Link-Training Quality	Stability improved through controlled board tests	Stronger link stability during load fluctuations [12]
Peripheral Alignment	Device mapping confirmed hardware–software match	Improved coordination and reduced mismatch faults

BVT helps identify the exact noise points across frequency bands, so designers can apply better filtering, improve routing, or adjust equalization to clean up the path [32]. Clean signals reduce retransmissions and raise total throughput. The link-training quality tests show that stability improves when boards operate under controlled conditions. Link training is the moment when the devices agree on how to talk to each other. If this moment is messy, the system starts on the wrong foot. BVT pushes repeated training cycles under temperature, power, and workload stress to expose unstable negotiation states. Once engineers understand the failure modes, they can refine firmware algorithms or tighten electrical constraints to make every link training round more stable [33].

4.8 Telemetry-Driven Fault Visibility Across Silicon Conditions

Telemetry-driven fault visibility targets using real-time data streams from silicon components to detect, explain and predict errors across varying operating conditions [34]. Thus, modern silicon runs under diverse voltage levels, thermal loads and workload-intensive environments that make faults more likely in behaviour dynamics.

$$Vfault=f(T1,T2,\dots,Tn / S)$$

Here Telemetry-Based Fault Visibility formula highlights that V_{\text{fault}} Vfault = visibility level of a fault

TiT_iTi = telemetry features (voltage, temperature, timing, error rates, etc.) SSS = silicon conditions (process variation, ageing, workload, thermal state)

f(⋅)f(\cdot) f(⋅) = function mapping telemetry + conditions to fault clarity

This formula provides fault visibility on multiple telemetry signals interpreted under specific silicon conditions. By combining these inputs, engineers gain clearer insight into hidden fault behaviors. Telemetry enables engineers to observe subtle degradations that conventional testing cannot detect [35]. Small timing drift, which highlights edge transitions and intermittent link issues, often remains hidden during static tests. Telemetry in place also exposes faults that only emerge under prolonged, high-stress conditions. These insights support stronger design choices.

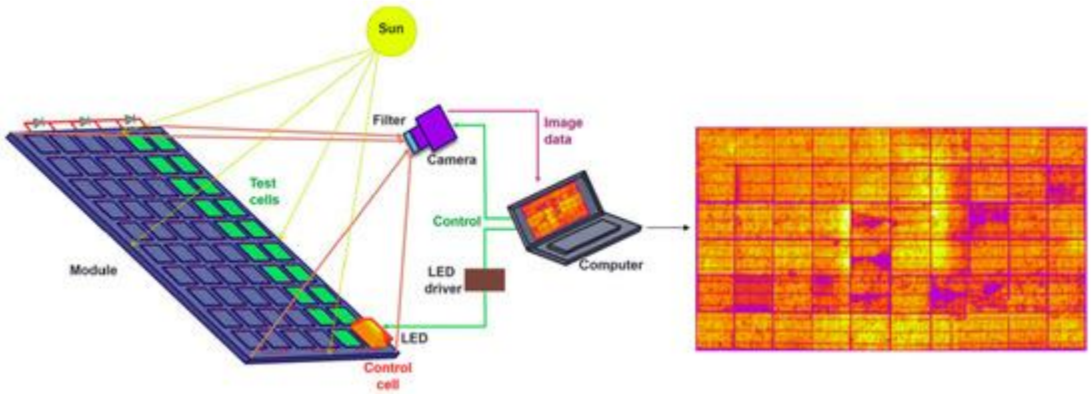

Figure 3: Enhanced PL imaging setup using optical filtering and current modulation [36]

Another key benefit is correlation. Telemetry connects with different data layers like thermal and logic events to form a complete picture of system health. Therefore, a burst of error-correcting code events might link to voltage instability. Such a correlation allows accurate root cause finding instead of guess-based debugging. Telemetry further enhances visibility by enabling cross-silicon comparison. Telemetry maps these differences and helps engineers understand variations that affect performance and visibility. However, multiple learning adds more power to telemetry-driven visibility [37]. This makes it easier to catch them before they grow into major failures. Predictive analytics supports practice maintenance and reduces downtime.

4.9 Predictive Failure Forecast Using Machine-Learning Models

Predictive failure uses machine learning models to estimate when hardware faults are likely to occur by studying patterns in operational data [38]. Modern silicon devices generate large volumes of elementary particles, which provide voltage shifts, thermal trends and clock variations. Machine learning models analyze these signals to detect early warning signs which appear before a visible failure.

Table 17: Machine-Learning–Driven Predictive Failure Forecasting

Process Stage	**Data Input**	**ML Technique**	**Forecast Output**	**Operational Value**
Data acquisition	Sensor logs	Feature extract	Early anomaly	Baseline insight
Pre-processing	Clean signals	Noise filter	Stable patterns	Model readiness
Model training	Labeled sets	Regression/NN	Failure score	Predict accuracy
Model inference	Live streams	Real-time classify	Risk estimate	Rapid response
Validation cycle	Test batches	Error analyze	Reliability check	Deployment trust

Models like random forests, gradient boosting systems and support vector machines that learn about normal behavior differ from abnormal drift. Moreover, a key strength of machine learning forecasting is its adaptability across silicon conditions. Chips behave very differently under varying workloads, temperatures, voltages and ages. Traditional threshold-based monitoring fails to cover dynamic scenarios [39]. A key strength of machine learning forecasting is its adaptability across silicon conditions. Traditional threshold-based monitoring fails to cover these dynamic scenarios. ML models are adjusting specific predictions based on real-time data. Predictive forecasting supports early interventions. Systems switch workloads, adjust power settings and trigger automatic routines before damage escalates.

$$\mathbf{F\hat{}(t)=M(T1(t),\ T2(t),\ldots,Tn(t))}$$

Here, the above formula highlights that—

F^(t) = predicted failure probability at time t

M(·)M(\cdot) M(·) = trained machine-learning model

Ti(t)T_i(t) Ti(t) = telemetry features at time t

The above formula highlights that probability is predicted by feeding multiple telemetry signals into a trained ML model. Each of the included features represents real-time behavior, and the models learn about specific patterns linked to early fault signatures.

Predictive failure forecasting uses machine-learning models to detect fault patterns long before hardware degradation becomes visible. Unlike static thresholds, ML systems learn evolving behaviour under shifting voltage, temperature and workload conditions. These models analyse telemetry streams—such as thermal drift, timing jitter and power fluctuation—to classify subtle deviations that indicate rising failure probability. Techniques like random forests, gradient boosting and neural networks adapt to device ageing and workload variance, producing dynamic risk scores. Their predictions enable proactive mitigation, including workload balancing, voltage tuning and thermal stabilisation. This early action reduces catastrophic faults, improves silicon lifespan and enhances overall system reliability.

Table 18: Table: Ensemble-Driven Predictive Failure Forecasting Framework

Stage	Data Source	Key Signal	ML Process	Output Metric	Action Trigger	Operational Benefit
Telemetry fusion	Multi-subsystems	Cross-domain drift	Signal merging	Unified profile	Anomaly flag	Higher precision
Correlation scan	Thermal logs	Timing skew	Pattern detect	Risk cluster	Alert generate	Early warning
Continuous learning	Long-term data	Behaviour shifts	Model update	Boundary refine	Score adjust	Adaptive accuracy
Instability scoring	Live telemetry	Stress markers	Risk scoring	Component rank	Debug direct	Targeted fixes
Focused diagnostics	Subsystem traces	Fault cues	Issue isolate	Root cause	Patch execute	Less overhead
Lifecycle planning	Historical sets	Age effects	Trend analyse	Degradation map	Plan optimise	Strong resilience

Predictive failure forecasting also benefits from ensemble-driven monitoring pipelines that merge telemetry from multiple subsystems to enhance diagnostic precision. Machine-learning classifiers recognize cross-domain correlations—such as simultaneous thermal rise and timing skew that reliably precede latent degradation. These models refine predictions through continuous learning, updating risk boundaries as silicon behavior evolves over months of operation. Adaptive scoring highlights components approaching instability, enabling targeted debugging rather than broad system-wide tests. This focused intervention reduces engineering overhead, cuts validation time and supports smarter lifecycle planning. By integrating ML-driven foresight with hardware self-checks, organizations achieve more resilient and maintainable silicon infrastructures.

5. Discussion:

Early hardware bring-up is the stage where a new semiconductor chip first comes alive outside the design environments. It is the significant moments where designers move from theory to real behavior. EVT (Engineering Validation Test) and BVT (Board Validation Test) form the main engineering of this early process [40]. EVT and BVT help check if the chip behaves as expected, if the signs move correctly and if the system works when all parts come together. In EVT, engineers focus on the core silicon. The EVT exposes problems like weak power rails, timing margins that collapse under load, and faulty logic blocks. The value of EVT is that it shows the true behavior of the silicon before the board system influences it. BVT checks if communication links behave normally, which supports clean signal flow, and if timing between the chip and peripherals stays stable. Bring up teams to test signals like PCIe, DDR, USB and internal buses. The bridge between design and real functionality becomes strong when EVT and BVT are combined [41]. EVT targets the silicon. The goal is to understand how the chip performs in raw form without external influences. Engineers measure power integrity, voltage response and timing accuracy. They verify logic and execute correctly; security blocks activate as designed and internal buses behave within defined limits. Engineers check if the board routing helps clean signal paths, if connectors maintain alignment and if interface protocols remain stable under load. BVT reveals issues like drops, termination mismatches, and noises. It's the systems of the chip that respond to real-world electrical environments. EVT includes certainty about silicon fundamentals, while BVT confirms systems integration [42]. Insights from the EVT guide board expectations and BVT findings help to improve firmware strategies. Problems discovered early are easier and cheaper to correct, which reduces the risk of redesigns and launch delays. Early hardware bring-up acts as the crucial bridge between chip design and real-world functionality. EVT checks whether the silicon behaves correctly under controlled electrical and logical conditions, allowing engineers to detect design mismatches before full system integration. BVT pushes the chip through practical workloads, revealing timing drift, thermal instability, and interface faults that only appear under sustained stress. Together, EVT and BVT expose hidden weaknesses that schematic simulations often miss. These validation phases help confirm that power delivery, signal paths, and subsystem interactions meet operational expectations. By combining structured diagnostics with real-environment testing, engineers ensure that early silicon matures into reliable and production-ready hardware. Moreover, EVT and BVT bring-up transform a theoretical design into a predictable, well-understood hardware platform. It ensures that fundamental blocks, signal paths, and system interfaces align with engineering goals.

6. Conclusion:

The combined use of EVT and BVT creates a strong pathway for turning semiconductor designs into fully functional systems. EVT establishes confidence in the silicon by strongly validating its electrical behavior, timing accuracy and internal logic stability. BVT extends expensive stages of development by testing the chip's performance on the actual board, interface and peripheral components. Here this research includes engineers with a complete understanding of both the chip and its operational environments. The clear separation of silicon-level and board-level evaluation, which allows efficient debugging improvements. This coordination reduces development risks, avoids costly redesigns and strengthens overall reliability. All over, EVT and BVT bring up a crucial bridge between design intention and real hardware performance. This leads to a stronger, more stable semiconductor platform ready for integration, mass production and long-term use.

Reference

1. J. R. Raja, A. Kella, and D. Narayanasamy, “The essential guide to computer system validation in the pharmaceutical industry,” *Cureus*, vol. 16, no. 8, 2024. [Online]. Available: https://www.cureus.com/articles/279102-the-essential-guide-to-computer-system-validation-in-the-pharmaceutical-industry.pdf
2. Instrumental.com, “EVT, DVT, PVT Stage Gate Definitions,” 2023. [Online]. Available: https://instrumental.com/build-better-handbook/evt-dvt-pvt
3. E. Perdomo *et al.*, “Makinote: An fpga-based hw/sw platform for pre-silicon emulation of risc-v designs,” in *Proc. 16th Workshop Rapid Simulation Performance Evaluation Design*, 2024, pp. 29–34. [Online]. Available: https://dl.acm.org/doi/abs/10.1145/3642921.3642928
4. J. A. Belloch *et al.*, “Evaluating the computational performance of the xilinx ultrascale+ eg heterogeneous mpsoc,” *Journal of Supercomputing*, vol. 77, no. 2, pp. 2124–2137, 2021. [Online]. Available: https://link.springer.com/article/10.1007/s11227-020-03342-7
5. Fortune Business Insights, “Semiconductor Market Size & Share | Industry Growth [2020–2027],” 2022. [Online]. Available: https://www.fortunebusinessinsights.com/semiconductor-market-102365
6. A. J. Miles, S. G. Ramalli, and B. A. Wallace, “DichroWeb, a website for calculating protein secondary structure from circular dichroism spectroscopic data,” *Protein Science*, vol. 31, no. 1, pp. 37–46, 2022. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pro.4153

7. N. Azliana Aridi, T. Siow Hooi, and C. Wen Cheong, "A comparative VaR analysis between low-frequency and high-frequency conditional EVT models during COVID-19 crisis," *Cogent Economics & Finance*, vol. 12, no. 1, p. 2377495, 2024. [Online]. Available: https://www.tandfonline.com/doi/abs/10.1080/23322039.2024.2377495
8. [C. Herzog and P. Kelly, "Applying thematic analysis to analyse press coverage in cross-country comparative research: A qualitative study protocol," *Int. J. Qualitative Methods*, vol. 22, 2023. [Online]. Available: https://books.google.com/books?hl=en&lr=&id=M2R2EAAAQBAJ&oi=fnd&pg=PA76&dq=thematic+analysis+supports+comparing&ots=NVbpoY7A0_&sig=7CH8SvFEGXeavuFeYO8-1lJ7WNA
9. Z. Chen *et al.*, "VoltPillager: Hardware-based fault injection attacks against intel SGX enclaves using the SVID voltage scaling interface," in *Proc. 30th USENIX Security Symp.*, 2021, pp. 699–716. [Online]. Available: https://www.usenix.org/conference/usenixsecurity21/presentation/chen-zitai
10. A. Chakraborty *et al.*, "Engineering multifunctional adhesive hydrogel patches for biomedical applications," *Interdisciplinary Medicine*, vol. 1, no. 4, p. e20230008, 2023. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/INMD.20230008
11. P. He *et al.*, "State-Space Dynamic Functional Regression for Multicurve Fixed Income Spread Analysis and Stress Testing," *arXiv preprint arXiv:2409.00348*, 2024. [Online]. Available: https://arxiv.org/abs/2409.00348
12. A. A. B. Mahathir *et al.*, "Advancements in IoT-Based Healthcare Monitoring and Memory Hierarchy in Computing," 2025. [Online]. Available: https://www.preprints.org/frontend/manuscript/db6596cdf8ed5c860d447e5c1d43846d/download_pub
13. H. Ma, C. Yi, and C. Wu, "Review and outlook on durability of engineered cementitious composite (ECC)," *Construction and Building Materials*, vol. 287, p. 122719, 2021. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0950061821004797
14. Liu Q, Wang J, He L. Reducing Mortality in AIS Patients After EVT: Challenges and Prospective Strategies [Response to Letter]. Clinical Interventions in Aging. 2025 Dec 31:213-5. https://www.tandfonline.com/doi/full/10.2147/CIA.S521480
15. Purraji M, Zamiri E, Sanchez A, de Castro A. Rapid Prototyping for Design and Test of FPGA-Based Model Predictive Controllers for Power Converters. Journal of Electrical Engineering & Technology. 2025 Feb 24:1-20. https://link.springer.com/article/10.1007/s42835-025-02173-x
16. Azliana Aridi N, Siow Hooi T, Wen Cheong C. A comparative VaR analysis between low-frequency and high-frequency conditional EVT models during COVID-19 crisis. Cogent Economics & Finance. 2024 Dec 31;12(1):2377495. https://www.tandfonline.com/doi/abs/10.1080/23322039.2024.2377495
17. Vilardell S, Rossi F, Giordana G, Serra I, Mezzetti E, Abella J, Cazorla FJ. Probabilistic Timing Estimates in Scenarios Under Testing Constraints. InProceedings of the 40th ACM/SIGAPP Symposium on Applied Computing 2025 Mar 31 (pp. 560-569). https://dl.acm.org/doi/abs/10.1145/3672608.3707895
18. Cock D, Ramdas A, Schwyn D, Giardino M, Turowski A, He Z, Hossle N, Korolija D, Licciardello M, Martsenko K, Achermann R. Enzian: an open, general, CPU/FPGA platform for systems software research. InProceedings of the 27th ACM International Conference on Architectural Support for Programming Languages and Operating Systems 2022 Feb 28 (pp. 434-451). https://www.researchgate.net/profile/Qian-Ma-77/publication/359573731_FPGA-based_accelerator_for_object_detection_a_comprehensive_survey/links/634d34c39cb4fe44f32fad3d/FPGA-based-accelerator-for-object-detection-a-comprehensive-survey.pdf
19. Li X, Lu P, Zhu R, Ma Z, Cao J, Xue JH. Rise by lifting others: Interacting features to uplift few-shot fine-grained classification. IEEE transactions on circuits and systems for video technology. 2024 Nov 18. https://ieeexplore.ieee.org/abstract/document/10756726/
20. Laksono ED. Analysis Of Mean Time Between Failure (MTBF) On Oil Production Machines. Jurnal Multidisiplin Sahombu. 2025 Jun 30;5(04):851-61. https://ejournal.seaninstitute.or.id/index.php/JMS/article/view/6889
21. Sashidhar D, Kwok H, Coult J, Blackwood J, Kudenchuk PJ, Bhandari S, Rea TD, Kutz JN. Machine learning and feature engineering for predicting pulse presence during chest compressions. Royal Society Open Science. 2021 Nov 10;8(11):210566. https://royalsocietypublishing.org/doi/abs/10.1098/rsos.210566
22. Rehberg L, Brem A. Bridging the gap: Linking prototyping and technology readiness levels for integrative product development. Creativity and Innovation Management. 2025 Mar;34(1):237-52. https://onlinelibrary.wiley.com/doi/abs/10.1111/caim.12633
23. Wu Y, Wang J, Wang Y, Zhai S, Li Z, He Y, Sun K, Li Q, Zhang N. Your firmware has arrived: A study of firmware update vulnerabilities. In33rd USENIX Security Symposium (USENIX Security 24) 2024 (pp. 5627-5644). https://www.usenix.org/conference/usenixsecurity24/presentation/wu-yuhao
24. Chaiwong N, Rerkasem B, Pusadee T, Prom-u-thai C. Silicon application improves caryopsis development and yield in rice. Journal of the Science of Food and Agriculture. 2021 Jan 15;101(1):220-8. https://scijournals.onlinelibrary.wiley.com/doi/abs/10.1002/jsfa.10634
25. Mandya Channegowda MG. Improving time-to-market and customer satisfaction in the SoC product business: an approach to enhance productivity by "reusability strategy". https://www.theseus.fi/bitstream/handle/10024/754590/Mandya%20Channegowda_Madhusudhan%20Gowda.pdf?sequence=4

26. P. A. Pegoraro *et al.*, "Compensation of systematic errors for improved PMU-based fault detection and location in three-phase distribution grids," *IEEE Trans. Instrum. Meas.*, vol. 73, pp. 1–12, 2024. [Online]. Available: https://www.researchgate.net/profile/Emmanuel-Echeonwu/publication/380632197...
27. S. Y. Wang, "Ensemble2: Anomaly Detection via EVT-Ensemble Framework for Seasonal KPIs in Communication Network," *arXiv:2205.14305*, 2022. [Online]. Available: https://arxiv.org/abs/2205.14305
28. V. Shah *et al.*, "Predictive Analytics for Traffic Management Systems," FHWA-HRT-24-091, 2024. [Online]. Available: https://rosap.ntl.bts.gov/view/dot/74275
29. [28] J. Vasconcelos *et al.*, "On vulnerabilities in EVT-based timing analysis," *Design Automation for Embedded Systems*, vol. 28, no. 1, pp. 1–21, 2024. [Online]. Available: https://link.springer.com/article/10.1007/s10617-023-09277-5
30. TMI, "Purpose-Built Power Analyzers for Precise EV Testing," 2025. [Online]. Available: https://tmi.yokogawa.com/library/resources/media-publications/purpose-built-power-analyzers-for-precise-ev-testing/
31. J. J. Badger *et al.*, "Incorporating telemetry information into capture-recapture analyses," *Methods Ecol. Evol.*, vol. 15, no. 10, pp. 1847–1858, 2024. [Online]. Available: https://besjournals.onlinelibrary.wiley.com/doi/abs/10.1111/2041-210X.14408
32. C. Morandotti *et al.*, "Non-invasive assessment of integrated cardiorespiratory network dynamics after physiological stress in humans," *J. Physiol.*, 2025. [Online]. Available: https://physoc.onlinelibrary.wiley.com/doi/abs/10.1113/JP288939
33. R. Nagulapalli, "Low power and high signal to noise ratio bio-medical AFE design techniques," Ph.D. dissertation, Oxford Brookes Univ., 2023. [Online]. Available: https://radar.brookes.ac.uk/radar/file/74e88470-f109-4f23-a355-db01028f36a1/1/Nagulapalli2023AFEdesign.pdf
34. M. Usman *et al.*, "Toward a more sustainable environment," *Human Resource Management*, vol. 62, no. 3, pp. 355–371, 2023. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/hrm.22148
35. V. Petrucci, F. Zacarias, and D. Roberts, "A Limits Study of Memory-side Tiering Telemetry," *arXiv:2508.09351*, 2025. [Online]. Available: https://arxiv.org/abs/2508.09351
36. D. R. Harbeck *et al.*, "Informing observatory operations with accessible telemetry," in *Proc. SPIE*, vol. 12186, pp. 289–300, 2022. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/12186/1218611/...
37. I. Polymeropoulos and S. Bezyrgiannidis, "Enhancing Solar Plant Efficiency," *Technologies*, vol. 12, no. 10, p. 175, 2024. [Online]. Available: https://www.mdpi.com/2227-7080/12/10/175
38. S. Nepal *et al.*, "Telemetry-Driven AI Agents," *Proc. ACM Hum.-Comput. Interact.*, vol. 9, no. 7, pp. 1–41, 2025. [Online]. Available: https://dl.acm.org/doi/abs/10.1145/3757408
39. M. C. van Rossum *et al.*, "Adaptive threshold-based alarm strategies for continuous vital signs monitoring," *J. Clin. Monit. Comput.*, vol. 36, no. 2, pp. 407–417, 2022. [Online]. Available: https://link.springer.com/article/10.1007/s10877-021-00666-4
40. D. Feng *et al.*, "Deep Learning and Adaptive Threshold-Based Signaling Storm Prediction," *IEEE Access*, vol. 11, pp. 120603–120611, 2023. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/10295468/
41. D. Laspisa *et al.*, "Mining the Utricularia gibba genome for insulator-like elements," *Frontiers Plant Sci.*, vol. 14, p. 1279231, 2023. [Online]. Available: https://www.frontiersin.org/journals/plant-science/articles/10.3389/fpls.2023.1279231/full
42. B. Pratap and P. Ragam, "LoRa Sense," *Computer Modeling Eng. Sci.*, vol. 142, no. 1, p. 425, 2025. [Online]. Available: https://cdn.techscience.press/files/CMES/2024/TSP_CMES-142-1/TSP_CMES_52355/TSP_CMES_52355.pdf
43. D. Eicke, "Hispanic students' postsecondary access and persistence," Ph.D. dissertation, 2021. [Online]. Available: https://ttu-ir.tdl.org/items/3bf1ccba-1257-404d-892f-1e1bd381e66e