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Article

Low Power Optimization of Hybrid Logic Full Adder Design using FinFET Technology for High-Speed Arithmetic Circuits

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Abstract: —Power efficiency and high computational speed are the necessary requirements in present-day digital processors for use in artificial intelligence hardware, edge computing platforms, and mobile devices. The traditional arithmetic logic circuit designs, based on CMOS transistors, face the issues of having high leakage currents, poor power efficiency, and reduced effectiveness in deep nanometer technology nodes. In this paper, an attempt is made to address the above problem by designing a low power hybrid logic full adder circuit with an approach of Pass Transistor Logic Adder Circuit implemented using FinFET transistors. Better electrostatic control and reduced short channel effect makes FinFET transistors an ideal choice for improving the performance of electronic circuits. Simulations done with HSPICE software show that the proposed adder circuit design outperforms the existing GNRFET technology by achieving 94.8%, 93.6%, 60.2%, 97.9%, and 68.5% improvements in power dissipation, current consumption, propagation delay, power-delay product, and average power dissipation respectively.
Keywords: —FinFET Technology; Hybrid Logic Full Adder; Pass Transistor Logic Adder; Low Power VLSI Design; HSPICE Simulation; Nano-scale Arithmetic Circuits; Energy Efficient Digital Systems.

1. Introduction

With the growing development of digital computing systems, the demand for arithmetic circuits that guarantee quick processing and energy efficiency is gaining importance. Adder is considered among the most essential components in the implementation of various arithmetic circuits for processors and digital signal processing systems. Notably, the functionality and design of the adder circuit play an integral part as the basic component in multipliers, arithmetic logic units, and other computing devices that rely on addition in their operations. Consequently, the performance of IC chips depends significantly on the attributes of the full adder, including power dissipation, propagation delay, and energy efficiency. Nonetheless, the growing tendency towards semiconductor miniaturization has led to several problems related to energy consumption and reliability in chip performance caused by leakage current, short-channel effects, switching activity, and other factors [1]-[5].

It is imperative to note that the employment of conventional CMOS transistors for the implementation of the adder circuit causes certain limitations associated with high power dissipation and significant leakage currents. Additionally, the switch performance is substantially impacted by modern CMOS transistor technology. Considering numerous drawbacks arising when implementing CMOS transistors in modern digital computing systems, it becomes critical to introduce new solutions for enhancing switching efficiency and reducing power dissipation. Specifically, in

recent years, much attention has been drawn to the utilization of graphene nanoribbon field-effect transistors due to their excellent features, including thermal stability and switching capability. Indeed, graphene nanoribbons have been expected to become an excellent material for future nanotechnology applications owing to these characteristics [1], [3], [6].

While optimizing transistor performance, it is equally vital to improve full adder design and performance. The use of hybrid transistors that combine pass transistor logic, complementary CMOS transistors, and transmission gate logic became popular due to outstanding switching performance. It is crucial to emphasize that pass transistor logic consumes less transistor overhead and dissipates less power than other transistor logic. Thus, the optimization of the XOR-XNOR logic circuitry, transistor design, and hybrid transistor logic can substantially impact the overall performance and energy efficiency of modern adders [4], [5], [7], [10], [11].

Despite numerous advances in designing advanced hybrid pass transistor logic structures and transistor types that led to the creation of powerful adders, certain problems remain. For example, there is a noticeable increase in energy consumption in many existing adder designs due to high leakage currents. Additionally, the design of novel transistor types requires a unique architectural approach to implement circuits successfully owing to their distinctive attributes. Hence, the problem of developing and optimizing modern adders using novel transistor designs remains actual. The objective of this research paper is to design and optimize a hybrid full adder using FinFET technology in transistor-level simulations.

The novelty of this research project stems from the fact that the Pass Transistor Logic Adder circuit has been re-designed and enhanced in terms of its optimization regarding switching performance in the context of circuit operations via the design and simulation of a Hybrid 24T Full Adder Circuit using FinFET Technology using HSPICE in Transistor-Level Simulations. Earlier attempts to design and simulate similar logic circuits have concentrated primarily on the introduction of GNRFET devices to improve their switching performance. This research initiative aims to achieve the same target using FinFET devices while employing the same logic circuit architecture for utilizing the electrostatic control of the FinFET device to reduce leakage in nano-scale arithmetic circuits.

An additional innovative aspect of this research project involves the comparative analysis of GNRFET-Based Pass Transistor Logic Adder Circuits and FinFET-Based Pass Transistor Logic Adder Circuits regarding their behavior under the same conditions in the HSPICE simulation environment. The attributes that will be compared include Power Dissipation, Current Consumption, Propagation Delay, Power Delay Product, and Average Power Consumption.

2. Related Work

A lot of research works concerning the optimization of the low power adder design have been made throughout the last decade because of its relevance in VLSI systems operations. There were many methods proposed to enhance the performance of adders such as reduction of the transistor number in the circuit architecture, application of hybrid logic types and usage of innovative transistors in the circuitry. The use of pass transistor logic and 22 nm graphene nanoribbon field effect transistors in the full adder circuit resulted in better switching properties and low power consumption when compared with traditional designs. Implementation of trimodal operation strategy helped significantly reduce power dissipation and delay product as well as decrease leakage in the process of varying operating conditions. The reliability of the circuit was also guaranteed [1].

One more important issue that is widely studied in relation to VLSI system operations concerns the search for effective trade-offs to achieve both power dissipation reduction and high circuit performance in fast arithmetic operations with hybrid full adder circuits. Circuit architectures with the hybrid logic type consist of transmission gates, complementary CMOS logic and pass transistor logic and help to minimize the number of transistors and switches used in the structure. The analysis showed that careful configuration of the XOR/XNOR gates greatly contributed to the delay and power dissipation minimization in the hybrid adder architecture. This was achieved by the elimination of superfluous signal transitions and propagation enhancement [4], [7], [11].

Many studies focused on investigation of innovative technologies and circuit architectures to improve reliability of VLSI systems. Adders with graphene nanoribbon field effect transistors provide high mobility and superior electrostatics resulting in good switching and reduced leakage currents. One more interesting technology in this case involves ternary logic circuits which show great performance and high energy efficiency [3], [6], [8].

In addition, there have been many studies concerned with improvement of VLSI systems using innovative transistors. FinFET technology with a three-dimensional transistor configuration provides better gate control, prevents short-channel effects, and offers good switching properties and minimized power leakage. The analysis of the

performance of the digital circuits built with FinFET transistors revealed superiority of FinFETs in terms of delay reduction and minimized power consumption. Comparison of the delay and power consumption in full adders based on various logic types also proved that optimized transistor configuration plays an important role in enhancing circuit performance [2], [9], [12]–[15].

Some more research works concerned with optimization of delay and power dissipation in VLSI systems by utilizing various transistor and logic types. Comparative evaluation of different XOR/XNOR gates created with hybrid logic types showed significance of proper transistor configuration in the process of minimizing delay and power consumption. Studies devoted to characteristics and behavior of FinFET and hybrid logic type transistors also pointed out the necessity for co-optimization of delay and power [9], [13], [14], [15].

3. Proposed Work

The implementation of the above proposed 24T hybrid logic full adder is made at the transistor level by making use of Synopsys HSPICE simulation tool by implementing the proposed circuit structure of Fig. 1. Structure for the implementation of the full adder is made in such a way that sum and carry outputs are obtained by means of 24 transistor circuitry design using hybrid pass transistor logic and complementary logic functions. Logical operation among the three inputs namely A, B, and Ci takes place with the help of appropriate switch paths so that the internal nodes produce the necessary intermediate voltages for obtaining output voltages. Implementation of the FinFET-based design of the adder is made according to the principles of the PTLA design with the modification in the design of devices in order to provide better electrostatic performance and lesser leakage current with switching efficiency of transistors at nanoscale level.

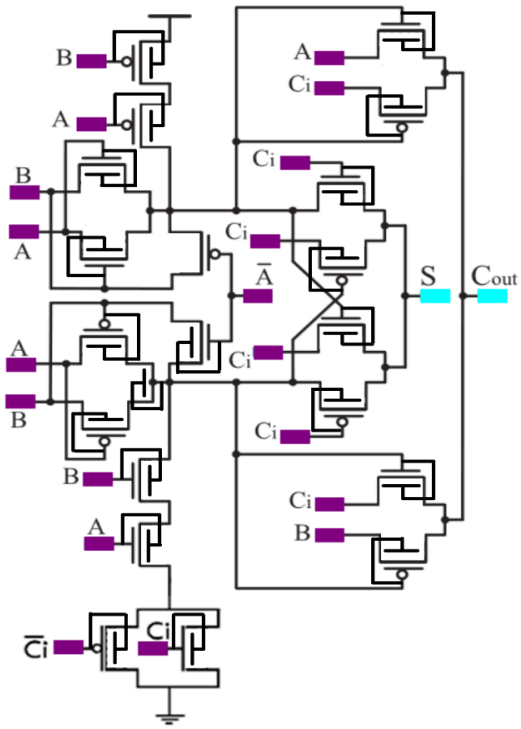

Fig. 1: 24T Adder using FinFET

Netlist definition for the adder circuit has been done by taking into account the transistor connections of the proposed 24T circuit. All the transistor sizes and input conditions have been specified in such a way that all the combinations of the input conditions have been taken into account for performing the transient analysis of the circuit. For FinFET-based circuit of the adder, the FinFET model is incorporated whereas for GNRFET-based PTLA, the GNRFET model is incorporated to develop the circuit for reference. The same input pattern and supply conditions

have been applied for transient analysis of both the circuits in order to observe the results for the same time duration so that the difference could only be observed due to difference in the technology.

Pulse stimulus inputs are applied to the circuit to observe all the switching events that are required for realization of the adder. The transient analysis has been performed in such a way that waveforms of the internal nodes, Sum output, and Carry output of the circuit are obtained. The rationale behind the choice of this method of analysis is that it not only gives the logical behavior of the circuit but also the dynamic performance of the adder circuit. As internal nodes play an important role in case of hybrid logic adder circuit, it is very important to avoid any signal distortion in order to get improved transitions which have been possible due to better gate-channel coupling provided by FinFETs.

Transient simulation for both the designs namely 24T Full Adder design and GNRFET-based PTLA design has been done with the help of HSPICE simulator. Since the simulation of both the circuits has been done at transistor level, all the electrical parameters of the circuit have been obtained through waveforms analysis. Transient analysis of the circuits has been done in order to obtain the necessary electrical characteristics of the circuit including Power dissipation, Current, Propagation Delay, Power-Delay Product, and Average Power. Output observations are also done in the same manner in order to facilitate the comparison of the two designs. This has been done in order to evaluate the effect of change in technology from GNRFET to FinFET based design.

The goal of the present implementation is not only to prove the functionality of the 24T Full Adder but to analyse whether the performance of the adder has been improved due to FinFET devices. Since full adders are extensively used in many arithmetic operations, even a minor change in the performance of the adder could greatly increase the efficiency of the arithmetic circuit. Thus, special consideration has been given in simulating the circuit with digital switching conditions with FinFET based design of the adder. With the help of this simulation methodology, effect of lesser short channel effects and leakage currents in the operation of the circuit has been observed.

In this way, whole process of implementation includes circuit design, incorporation of the transistor models into the design, pulse stimuli application and finally observation of the waveforms for determining the electrical parameters of the circuit. Thus, the proposed 24T Full Adder design has been implemented successfully at the transistor level through the help of Synopsys HSPICE software.

4. Results

The results of the transient simulations performed in the HSPICE environment have indicated successful operation of the proposed 24T hybrid logic full adder implemented using FinFET technology. As illustrated in Fig. 2 below, the waveforms representing the input signals have demonstrated that Sum and Carry signals respond in line with the fundamental logic of a one bit full adder. Input signals, namely A, B and Ci signals were used in the form of periodic pulses to evaluate all possible logical states of the circuit during the time period of simulation.

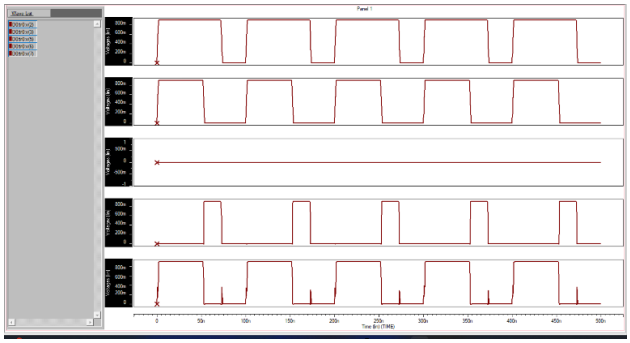

Fig.2: Waveform for 24T Adder using FinFET

From the analysis of the waveforms, it can be concluded that the responses in Sum and Carry signals are performed according to the expected logic of a full adder. Therefore, successful switching of the circuit has been achieved and implemented successfully. Moreover, it can be noted that there are no noticeable distortions observed during the transition from one logic state to another, indicating smooth transition and switching of the FinFET based PTLA.

In addition to the above-mentioned observations, due to excellent gate control capability of FinFET based transistors, voltage levels in the internal nodes in the circuit remain stable while transitioning through the logic circuit.

In addition, FinFET based pass transistors demonstrate stable logic level transition which allows the circuit to switch properly.

Table 1 Comparative Results for PTLA for GNRFET and FinFET

	FIN PTLA	GNR PTLA
Power Dissipation (W)	2.25E-12	4.35E-11
Current (A)	3.07E-12	4.83E-11
Delay (s)	2.62E-11	6.59E-11
PDP (J)	5.91E-23	2.86E-21
Average Power (W)	7.65E-11	2.43E-10

Table 1 below provides quantitative parameters of the circuit performance extracted from the transient simulations carried out in the HSPICE environment. According to Table 1, it can be concluded that there are considerable improvements achieved in the electrical performance of the circuit implemented in FinFET technology compared with the circuit implemented using GNRFET devices. Improvements in such parameters as power dissipation, current consumption, propagation delay, power delay product and average power consumption have been observed in the results. All the mentioned parameters have been obtained after transient simulations carried out on two different designs based on two different transistor technologies.

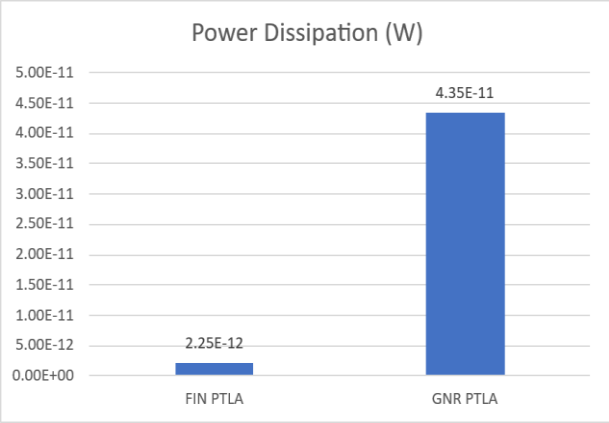

Fig. 3 Power Dissipation for 24T PTLA

Figure 3 illustrates results concerning power dissipation obtained after simulations performed on the circuits based on two different transistor technologies. From Figure 3, it can be seen that the proposed FinFET PTLA design consumes considerably lower energy than the circuit built in GNRFET technology. According to the obtained results, FinFET based PTLA circuit consumes 2.25E-12W while the GNRFET based adder consumes 4.35E-11W. Reduced power consumption is provided by better electrostatic control and low leakage current in FinFET technology.

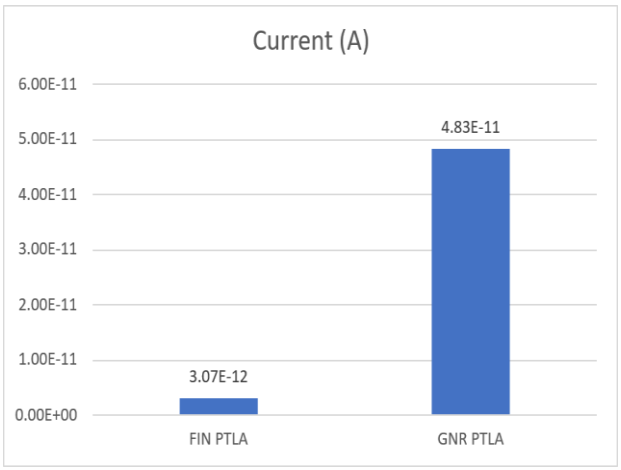

Fig. 4 Current for 24T PTLA

Figure 4 shows the comparison results of the current consumption of circuits implemented in FinFET and GNRFET technology. From the figure, it can be seen that the total current flow through the FinFET based design is significantly lower comparing to the total current consumed by the circuit designed with GNRFET technology. FinFET circuit consumes 3.07E-12A of current flow while GNRFET consumes 4.83E-11A.

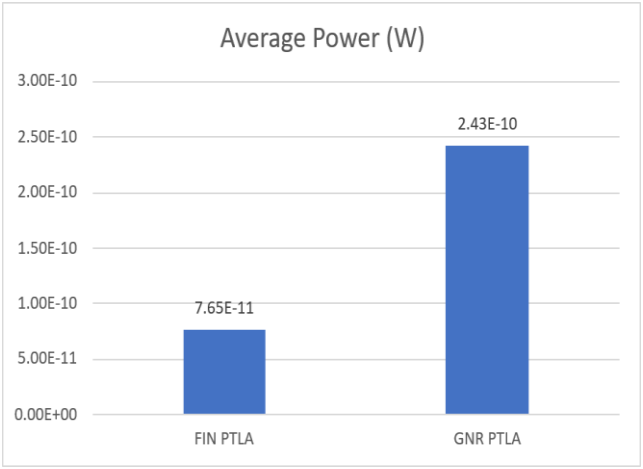

Fig. 5 Average Power Consumption 24T PTLA

Figure 5 illustrates average power consumption comparison results obtained for FinFET and GNRFET circuits. From the obtained results, it can be concluded that FinFET design consumes considerably less energy. Average power consumption for FinFET based circuit equals to 7.65E-11W while the same parameter equals to 2.43E-10W for GNRFET adder circuit. Reduced average power consumption is provided by improved electrostatic control and switching capability of the circuit.

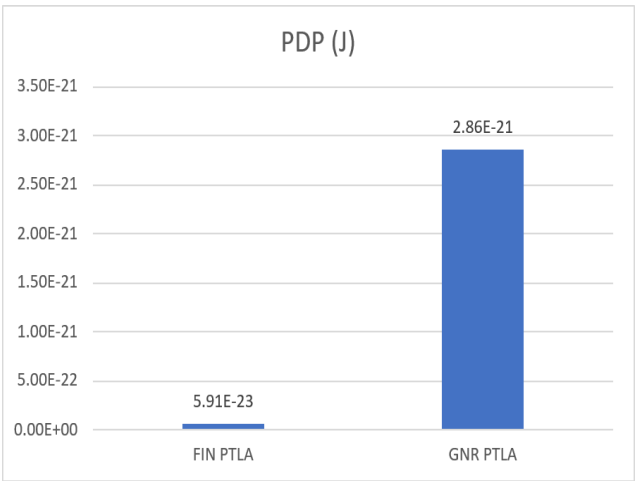

Fig. 6 PDP 24T PTLA

Figure 6 illustrates power delay product comparison results for the proposed FinFET design and the GNRFET counterpart. From Figure 6, it can be seen that FinFET PTLA requires lower energy consumption compared with the GNRFET based adder. FinFET circuit's power delay product equals to 5.91E-23J while GNRFET circuit's equal to 2.86E-21J. Power delay product defines the energy required for the switching event to occur in digital circuits.

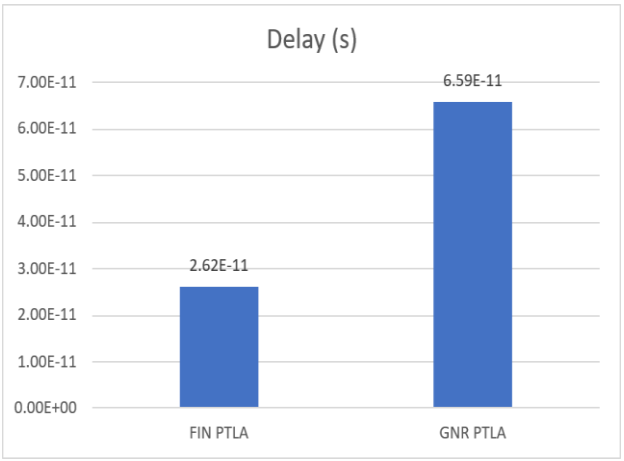

Fig. 7 Delay 24T PTLA

As depicted in Fig. 7 below, it is apparent that the proposed FinFET-based PTLA provides better results in terms of switching than the GNRFET-based PTLA. In FinFET-based PTLA, the propagation delay is determined to be 2.62E-11 seconds, whereas for GNRFET-based PTLA, the propagation delay is estimated at 6.59E-11 seconds. Propagation delay is critical for fast arithmetic circuits, as the propagation delay of full adder impacts the performance of arithmetic circuits such as ripple carry adder, multiplier, and ALU of processors.

5. Conclusion

The main focus of the research paper was on the proposed low power 24T hybrid logic full adder designed using the technology of FinFET devices. This design was compared with other existing design with respect to their electrical characteristics where the GNRFET based PTLA design was used for comparisons. The simulation results showed that the energy efficiency of both designs was significantly different. In this context, it is evident that the amount of energy used in FinFET based design was 94.8% less than GNRFET design. Additionally, there was a 93.6% difference in their current consumption. The delay was also significantly low in FinFET based design (60.2%). Consequently, the power-delay product of FinFET based design was increased by 97.9%, hence, more energy efficiency. The average power consumption was decreased by 68.5%.

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