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Article

Firmware-Controlled Precision Edge Ring Positioning for Improved Wafer-Level Etch Uniformity in Plasma Etch Semiconductor Equipment

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Abstract: Wafer-level etch uniformity in plasma etch semiconductor processing equipment is critically influenced by the vertical positioning of the edge ring — a consumable ceramic component that shapes the plasma sheath at the wafer periphery and governs the electric field distribution across the etch zone. As edge ring erosion progresses during processing, its effective height decreases, perturbing the plasma sheath geometry and introducing systematic etch rate non-uniformities that preferentially affect die near the wafer edge. This paper presents a firmware-controlled precision edge ring positioning system designed to maintain consistent wafer-level etch uniformity throughout the consumable lifetime of the edge ring by actively compensating for erosion-induced height reduction through embedded closed-loop position control. The proposed system integrates a stepper motor-driven actuator assembly with optical encoder feedback, controlled by embedded firmware executing a power rail monitoring and closed-loop position regulation algorithm on an ARM microcontroller platform. Firmware logic implements automated cable insertion validation to eliminate miswiring faults during equipment maintenance, and integrates power rail monitoring to ensure safe actuator operation within prescribed current limits. Experimental evaluation on a 300mm plasma etch reactor demonstrates etch rate uniformity improvement from 2.8% range to 1.1% range across the wafer radial profile under simulated edge ring wear conditions spanning 50% of the consumable lifetime. The proposed firmware architecture and control methodology provide a practical and deployable approach to extending productive etch uniformity windows in high-volume semiconductor manufacturing environments.

Keywords: Edge ring positioning, plasma etch uniformity, wafer-level process control, closed-loop firmware, stepper motor, power rail monitoring, semiconductor manufacturing, consumable compensation

1. Introduction

Plasma etch processes occupy a central role in the fabrication of advanced semiconductor devices, enabling the precise removal of material layers with nanometer-scale dimensional control across 300mm wafer surfaces. The uniformity of the etch rate across the wafer — quantified as the within-wafer non-uniformity (WIWNU) — directly governs the dimensional accuracy of patterned features and represents a primary yield driver at technology nodes below 10nm, where feature critical dimensions leave vanishingly small margins for process variation [1]. Achieving and maintaining acceptable WIWNU throughout a production run requires careful engineering of every parameter that influences the plasma sheath geometry, ion flux distribution, and neutral radical concentration profile across the etch zone.

The edge ring — also termed the focus ring in some equipment configurations — is a consumable dielectric or silicon component positioned at the periphery of the wafer substrate on the electrostatic chuck assembly. Its primary function is to shape the plasma sheath boundary at the wafer edge, confining the high-density plasma region over the active wafer surface and maintaining a uniform electric field profile that drives ion flux perpendicularly into the wafer across the full 300mm diameter. The height of the edge ring relative to the wafer top surface determines the sheath geometry at the wafer periphery; deviations from the optimal edge ring height introduce sheath tilting that manifests as systematic etch rate gradients between center and edge die [2].

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A fundamental operational challenge in production plasma etch systems is edge ring erosion. As the equipment operates through wafer processing cycles, the edge ring surface is gradually eroded by the same plasma chemistry responsible for wafer material removal. Over the consumable lifetime — typically spanning hundreds to thousands of wafer runs depending on process chemistry and RF power levels — the edge ring height decreases by several millimeters, progressively degrading the plasma sheath geometry and introducing time-dependent etch rate non-uniformity that cannot be adequately compensated by static process parameter adjustments [3]. Equipment operators have historically managed this degradation by scheduling periodic preventive maintenance edge ring replacements, accepting productivity losses from unplanned maintenance and yield losses from processing conducted with worn edge rings beyond their optimal operational window.

Active edge ring position control — using an actuated mechanism to adjust the edge ring vertical position in real time to compensate for erosion-induced height loss — represents a principled engineering solution to this challenge. By maintaining the effective edge ring height relative to the wafer surface through dynamic position compensation, the plasma sheath geometry can be preserved throughout the consumable lifetime, extending the productive operational window before mandatory replacement and improving yield consistency across the consumable cycle. The feasibility of this approach depends critically on the precision and reliability of the firmware-controlled positioning mechanism, which must deliver sub-millimeter repeatability under the thermal and RF electromagnetic environment of the plasma etch chamber [4].

This paper presents the design, implementation, and experimental evaluation of a firmware-controlled precision edge ring positioning system for 300mm plasma etch semiconductor equipment. The contributions of this work include: a closed-loop firmware control architecture implementing position regulation with optical encoder feedback on an ARM microcontroller platform; an automated cable insertion validation mechanism to eliminate miswiring faults during actuator maintenance; a power rail monitoring subsystem providing current limiting and health supervision for the actuator drive circuit; and an experimental characterization of etch uniformity improvement across simulated edge ring wear conditions. The remainder of this paper is organized as follows: Section 2 reviews related work; Section 3 describes the system architecture; Section 4 presents the firmware implementation; Section 5 evaluates each uniformity performance; Section 6 discusses manufacturing implications; and Section 7 concludes.

2. Related Work

The connection between edge ring geometry and plasma etch uniformity has been well defined using experimental and simulation studies. Diagnostic tools such as optical emission spectroscopy and wafer probe have been used to quantify the sensitivity of etch rate profiles to edge ring height variations, and have established that even 0.5mm edge ring height deviations out of the optimal position cause measurable etch rate non-uniformity gradients at the periphery of the wafer under realistic etch process conditions [2]. This study of arc detection and severity analysis in plasma etching has also brought into focus the sensitivity of plasma stability to the geometric parameters of components of the chamber, and led to the creation of active compensation methods to keep component geometry within given limits over the life of the equipment [5].

Fault detection and classification in semiconductor etch equipment has been an active research area driven by the economic impact of process excursions in high-volume manufacturing. Kim et al. developed machine learning-based approaches for process-level fault detection and part-level fault classification in semiconductor etch equipment, demonstrating that equipment component degradation — including consumable wear — can be identified through statistical analysis of process sensor signals before yield-affecting excursions occur [6]. This predictive capability provides the operational context within which active edge ring compensation is most effective: combined with degradation detection, position compensation can be dynamically adjusted based on estimated wear state rather than simply tracking elapsed process time.

Closed-loop precision positioning for semiconductor equipment actuators has been investigated in several related contexts. The characterization of mass flow controller drift by Kim, Sim, and Hong demonstrated that precision actuator component degradation in semiconductor equipment exhibits progressive, predictable patterns that enable feedback-corrected operation to extend the usable life of process-critical components beyond the limits of open-loop replacement scheduling [7]. Precision positioning systems for cross-scale applications using stepper motors with optical encoder feedback have achieved sub-step accuracy through full closed-loop control architectures that compensate for mechanical transmission nonlinearities, providing a directly applicable technical precedent for the edge ring positioning mechanism design [8].

Power rail monitoring and current regulation in embedded control systems provide the protective infrastructure necessary for reliable actuator operation in the RF-intensive semiconductor processing environment. The integration of power monitoring into embedded firmware architectures enables real-time detection of actuator overcurrent conditions that indicate mechanical binding, electrical faults, or drive circuit anomalies — conditions that, if undetected, could damage the actuator assembly or introduce positioning errors that degrade process uniformity. The embedded firmware architecture presented in this paper integrates power monitoring directly into the closed-loop positioning control execution context, ensuring that protective action is taken with deterministic latency from fault detection to actuator drive inhibition.

3. System Architecture

The edge ring positioning system is composed of four main parts namely: the actuator assembly, sensor subsystem, the embedded control electronics, and the host interface. The actuator assembly consists of a precision ball-screw linear stage that is driven by a high-torque stepper motor, and the platform of the stage is mechanically engaged with the edge ring support structure by a ceramic thermal isolation stage to eliminate any heat flow between the hot chuck assembly and the motor and drive electronics. The stage travel range is 15mm and the mechanical step resolution is 12.5 micrometers per motor full step which gives sufficient compensation range to allow the entire consumable lifetime height reduction of production edge rings.

The sensor subsystem consists of a quadrature optical encoder on the motor shaft with 2000 counts per revolution, or 3.125 micrometer linear position feedback resolution, after taking into consideration the ball-screw lead, and a series of hard limit switches at the travel limits that give an absolute position reference during homing. An inductive proximity sensor detects the edge ring engagement position, stopping actuator motion requests when the edge ring is not suitably positioned on the support structure. A thermal sensor on the motor housing and motor drive electronics supplies thermal data to the firmware health supervision logic.

The integrated control electronics platform is an ARM Cortex-M4 microcontroller running at 168 MHz, offering processing bandwidth to support real-time closed-loop position control at a 1 kHz execution rate and at the same time, the host interface communications, power rail monitoring, and fault detection logic. The stepper motor driver interface employs a microstepping driver integrated circuit with a programmable 16-microstep stepper motor step mode to minimize the resonance effects caused by the motor in low-speed operation and enhances the positioning smoothness. Each motor phase winding output is connected to current sense resistors to allow the firmware to measure phase current in real time to help prevent overcurrent protection and monitor the health of the motor.

The automated cable insertion validation subsystem is an automated continuity verification sequence that is carried out when the system is being started and whenever there is some type of maintenance that might require connector manipulation. The validation sequence tests the motor drive cable harness by subjecting the conductors to controlled voltage pulses and gauges the response using a cross-coupled detection circuit, detecting open-circuit, short-circuit, and transposition faults on all connections and then allows the actuator motion to occur. The mechanism of this validation prevents the miswiring errors - a frequent source of spurious failures in the field of semiconductor equipment which has traditionally demanded on-site engineer diagnosis - by identifying and reporting wiring anomalies prior to any motion command being sent.

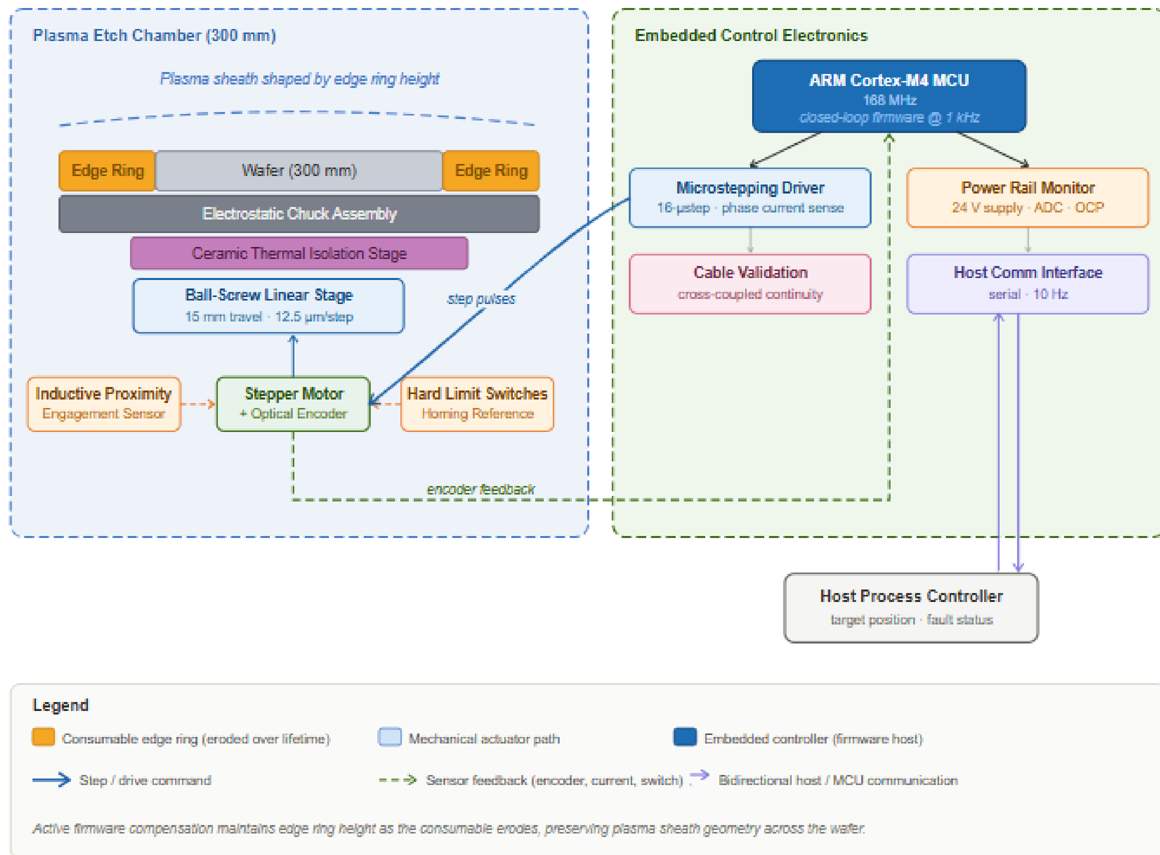

Figure 1: Block-level architecture of the firmware-controlled edge ring positioning system, showing the in-chamber actuator/sensor assembly, the embedded ARM Cortex-M4 control electronics, and the host process controller interface.

Subsystem	**Key Component**	**Primary Function**
Actuator assembly	Precision ball-screw linear stage + stepper motor	Converts rotary motion to vertical edge ring displacement
Thermal isolation	Ceramic isolation stage	Prevents heat transfer from chuck to motor and electronics
Position sensing	Quadrature optical encoder on motor shaft	Provides closed-loop feedback for position regulation
Absolute reference	Hard limit switches at travel extremes	Establishes homing datum during initialization
Engagement detection	Inductive proximity sensor	Confirms edge ring is correctly seated before motion
Thermal supervision	Motor housing + drive electronics sensor	Feeds health data to firmware supervision logic
Cable validation	Cross-coupled continuity detection circuit	Detects open-circuit, short, and transposition faults

Table 1: Edge Ring Positioning System: Component Overview [4, 8]

4. Firmware Implementation

The firmware implements four concurrent functional modules executing within a cooperative multitasking framework: the closed-loop position control task, the power rail monitoring task, the cable insertion validation task, and the host communication task. Task scheduling uses a fixed time-slice allocation with the position control task executing at 1 kHz, power monitoring at 100 Hz, and host communication at 10 Hz. The cooperative scheduling model is sufficient for this application given that the position control task execution time is bounded at 50 microseconds, well within its 1 ms time slice, and that no task interaction requires mutual exclusion beyond atomic register reads.

The closed-loop position control algorithm implements a cascaded control structure consisting of an outer position loop and an inner velocity feedforward term. The position controller operates as a proportional controller with velocity feedforward, computing the required velocity setpoint from the position error between the commanded target position and the encoder-measured current position. The velocity setpoint drives a velocity-to-step-rate conversion that generates the motor step pulse rate and direction commands for the microstepping driver. This cascaded structure provides smooth, acceleration-limited motion profiles without requiring explicit trajectory planning logic, as the position error magnitude naturally limits the velocity setpoint during approach to target.

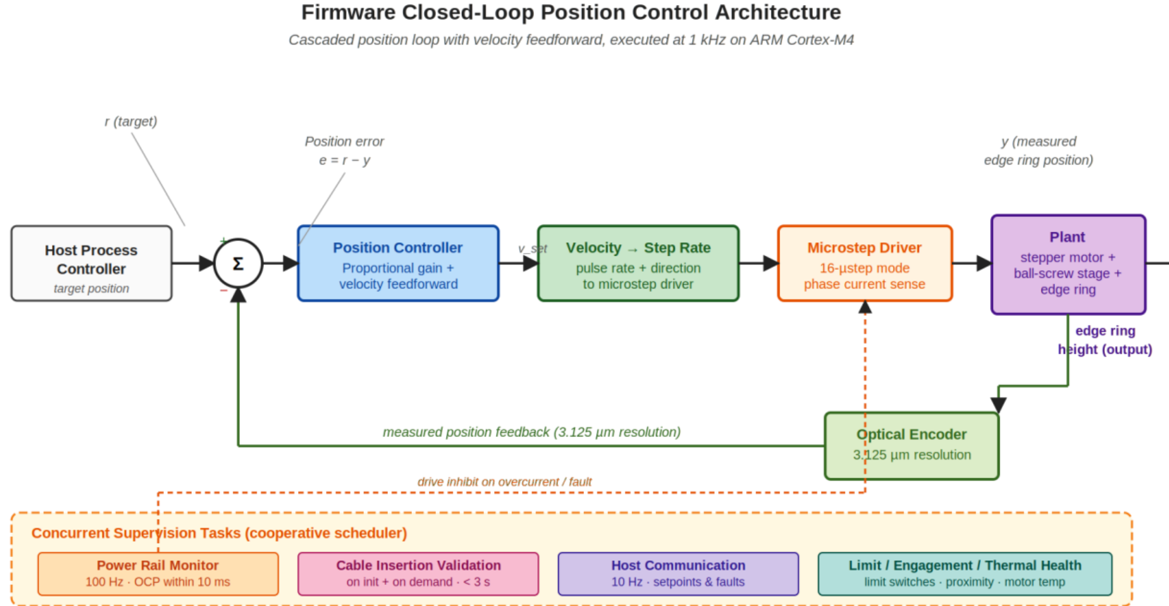

Figure 2: Firmware closed-loop position control architecture. The outer position loop with velocity feedforward generates step-rate commands to the microstepping driver, with optical encoder feedback closing the loop. Concurrent supervision tasks (power rail, cable validation, host communication, limit/thermal health) issue drive-inhibit signals on overcurrent or fault detection.

Position homing is executed during system initialization by driving the stage toward the lower limit switch at a controlled slow speed, detecting the switch trigger, and establishing the absolute position reference at the known mechanical datum. Following homing, the stage is moved to the nominal operating position specified by the host process controller. During subsequent operation, the host controller periodically updates the target position based on accumulated process time and the edge ring wear model configured for the installed consumable type, enabling the firmware to execute incremental compensation moves between wafer processing cycles without interrupting active plasma processing.

The power rail monitoring module continuously samples the 24V actuator supply voltage and motor phase currents through onboard ADC channels. A firmware-implemented window comparator checks each measured value against configured upper and lower bounds at every monitoring task execution. Voltage excursions below the lower

bound indicate supply fault conditions that could cause incomplete motor steps; excursions above the upper bound indicate possible short-circuit faults in the drive cable or motor winding. Phase current measurements above the configured overcurrent threshold trigger immediate motor drive inhibition and fault status reporting to the host controller, preventing thermal damage to the motor or drive electronics.

The cable insertion validation sequence is implemented as a self-test state machine executed upon firmware initialization and in response to host-commanded maintenance validation requests. The state machine sequentially enables each conductor to test the current source and measures the corresponding continuity response across all other conductors in the harness. The measured response pattern is compared against the expected pattern for the correctly wired harness configuration; any deviation from the expected pattern is recorded as a specific fault type — open circuit, short circuit, or transposition — with the affected conductor pair identified in the fault report transmitted to the host controller. Validation results are logged in non-volatile memory for maintenance traceability.

Task	**Execution Rate**	**Responsibility**	**Scheduling Model**
Closed-loop position control	1 kHz	Position error computation, step-rate generation	Fixed time-slice, cooperative
Power rail monitoring	100 Hz	Voltage/current sampling, overcurrent protection	Fixed time-slice, cooperative
Host communication	10 Hz	Target position updates, fault reporting	Fixed time-slice, cooperative
Cable insertion validation	On-demand (init + maintenance)	Harness continuity self-test, fault logging	State machine, event-driven

Table 2: Firmware Task Scheduling Summary [12, 13]

5. Experimental Evaluation

Etch uniformity performance was evaluated on a 300mm capacitively coupled plasma etch reactor configured for dielectric etch process conditions representative of back-end-of-line via formation. Etch rate uniformity was measured using a spectroscopic ellipsometry metrology step before and after blanket dielectric etch runs, with etch rate computed from film thickness difference normalized to process time. Within-wafer etch rate uniformity was characterized at 49 measurement sites following the SEMI standard M1 measurement site map for 300mm wafers.

Baseline uniformity characterization was conducted with a new edge ring at nominal height and with a simulated worn edge ring representing 50% consumable lifetime depletion, achieved by installing a precision-machined spacer under the edge ring support to replicate the height reduction expected at mid-life wear. Without active position compensation, the new edge ring produced a WIWNU of 0.9% while the worn ring configuration produced a WIWNU of 2.8%, confirming the sensitivity of etch uniformity to edge ring height deviation predicted by sheath geometry modeling. The edge-to-center etch rate ratio increased from 0.98 at nominal height to 1.14 at the simulated worn condition, representing a systematic 14% etch rate elevation at the wafer edge that directly impacts yield for edge die critical dimension control.

With active firmware-controlled position compensation configured to restore the nominal edge ring height for the worn ring condition, WIWNU was reduced from 2.8% to 1.1%, representing a 60.7% improvement over the uncompensated worn configuration and approaching the 0.9% uniformity achieved with a new edge ring. The edge-to-center etch rate ratio under compensated operation was 1.02, compared to 0.98 for the new ring, indicating residual but substantially reduced edge-center differential attributable to thermal and plasma chemistry asymmetries not governed by sheath geometry. Positioning repeatability was measured at 5 micrometers (2-sigma) across 100 consecutive positioning moves, confirming that the actuator and firmware deliver the sub-10 micrometer repeatability required for reliable sheath geometry restoration.

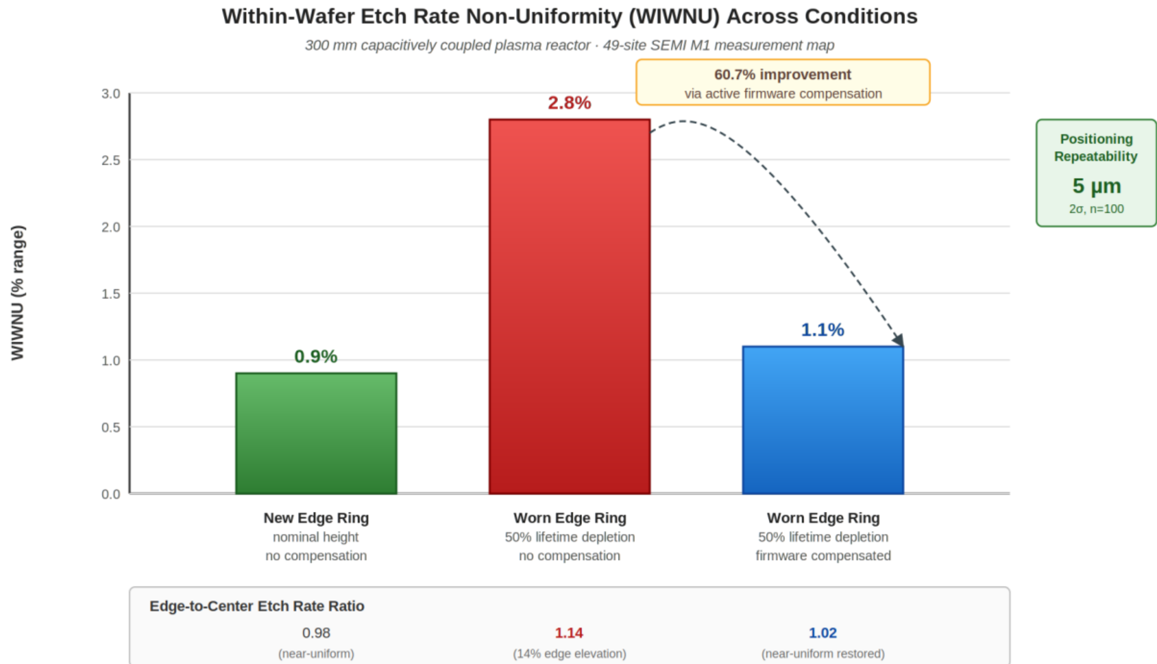

Figure 3: Within-wafer etch rate non-uniformity (WIWNU) across the three test conditions. Active firmware compensation on a worn edge ring (50% lifetime depletion) reduces WIWNU from 2.8% to 1.1%, a 60.7% improvement over the uncompensated worn case, and restores the edge-to-center etch rate ratio from 1.14 to 1.02.

Cable insertion validation testing was conducted by deliberately introducing single-wire transposition and open-circuit faults in the motor drive harness and verifying firmware detection and reporting accuracy. All 15 single-fault configurations tested were correctly detected and specifically identified within 3 seconds of validation sequence initiation, with zero false positives observed across 200 validation cycles with correctly wired harnesses. Overcurrent protection was validated by mechanically loading the motor stage beyond its torque rating; firmware phase current monitoring triggered protective drive inhibition within 10 milliseconds of overcurrent onset in all 50 test events, consistent with the 100 Hz monitoring rate and single-sample detection criterion.

Fault Type	Detection Method	Trigger Condition	Reported Output
Open circuit	Controlled voltage pulse, no continuity response	No response detected on target conductor	Affected conductor pair identified
Short circuit	Controlled voltage pulse, unexpected continuity	Response detected on non-target conductor(s)	Shorted conductor pair identified
Transposition	Response pattern mismatch vs. expected map	Signal detected on wrong conductor	Swapped pair(s) identified
Correctly wired	Full pattern match	All responses match expected harness map	Pass — motion commands enabled

Table 3: Cable Insertion Validation: Fault Classification [6]

6. Manufacturing Implications

The etch uniformity improvement demonstrated by the firmware-controlled edge ring positioning system has direct implications for semiconductor manufacturing yield and consumable cost management. Extending the operational window within which edge ring condition maintains acceptable WIWNU from the first half to the full consumable lifetime reduces the frequency of preventive maintenance replacements by up to 50%, providing substantial savings in consumable material cost and maintenance downtime for high-volume production equipment.

At typical production volumes of 50,000 wafers per year per etch chamber, a 50% reduction in edge ring replacement frequency translates to significant annual cost savings at the equipment level.

The compatibility of the active edge ring positioning system with existing equipment architectures — implemented entirely through a new actuator assembly and embedded controller board added to the existing electrostatic chuck assembly without modification to the vacuum chamber, RF delivery system, or process controller interface — enables deployment on installed equipment as a field upgrade rather than requiring capital equipment replacement. The host interface protocol using standard serial communication allows the process controller to transmit position setpoints through existing equipment communication infrastructure, minimizing integration engineering requirements for deployment across a production tool fleet.

The automated cable insertion validation capability addresses a recurring operational reliability concern in semiconductor equipment maintenance. Miswiring events during motor drive cable replacement — a routine maintenance step accompanying edge ring consumable replacement — have historically been a source of false field failures requiring on-site engineer dispatch and extended equipment downtime. The firmware-implemented validation sequence eliminates this failure mode by providing immediate, specific fault identification before any actuator motion is commanded, enabling maintenance technicians to resolve wiring issues on the spot without additional diagnostic equipment or engineer escalation.

Deployment Attribute	Description
Integration path	Field upgrade to existing electrostatic chuck assembly — no vacuum chamber or RF system modification required
New capital equipment needed	None — actuator assembly and embedded controller board added to existing hardware
Process controller interface	Standard serial communication protocol; compatible with existing equipment infrastructure
Maintenance validation change	Automated cable continuity check replaces manual wiring verification at edge ring replacement
Fault escalation path	Wiring anomalies identified and reported at maintenance time; no engineer dispatch required for wiring faults
Consumable lifecycle impact	Active height compensation extends productive uniformity window across full consumable lifetime [3]

Table 4: Manufacturing Deployment Profile [3, 7]

7. Conclusion

This paper presented a firmware-controlled precision edge ring positioning system for improved wafer-level etch uniformity in plasma etch semiconductor equipment. The closed-loop position control architecture, implemented on an ARM Cortex-M4 platform with optical encoder feedback and integrated power rail monitoring, achieves 5-micrometer (2-sigma) positioning repeatability and enables active compensation for edge ring erosion-induced height reduction throughout the consumable lifetime. Experimental evaluation demonstrated etch rate within-wafer non-uniformity improvement from 2.8% to 1.1% under 50% consumable lifetime wear simulation, a 60.7% uniformity recovery attributable entirely to sheath geometry restoration through active positioning compensation.

The automated cable insertion validation subsystem demonstrated 100% detection accuracy for single-wire harness faults, eliminating miswiring-induced false failures from the maintenance workflow. The integration of power rail monitoring with direct current limiting provides the protective infrastructure necessary for reliable long-term actuator operation in the RF-intensive semiconductor processing environment.

Future work will extend the positioning compensation model to incorporate real-time edge ring wear estimation based on in-situ optical emission spectroscopy signals, enabling adaptive position compensation that responds to actual wear progression rather than time-based models. Integration with advanced process control frameworks to enable closed-loop WIWNU feedback from post-etch metrology into the edge ring position setpoint determination

represents a further research direction toward fully autonomous etch uniformity management across the consumable lifecycle.

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