International Journal of Computer Information Systems and Industrial Management Applications.
ISSN 2150-7988 Volume 12 (2020) pp. 155-167

Received: 17 Jan, 2020; Accepted: 23 May, 2020; Published: 28 May, 2020

VLSI Implementation in Biomedical Applications: A Review

Nagavarapu Sowmya[1], Shasanka Sekhar Rout[2*] and Rajesh Kumar Patjoshi[3]

[1] Gandhi Institute of Engineering and Technology University,
Gunupur, India
nagavarapu.sowmya@gmail.com

[2*] Gandhi Institute of Engineering and Technology University,
Gunupur, India
ssrout1988@gmail.com

[3] National Institute of Science and Technology,
Berhampur, India
rajeshpatjoshi1@gmail.com

***Abstract*: Recent disastrous incidents in health care system have disturbed the continuous process of care, leaving the health care sector in a 'state of emergency'. The rise of trust flaw between patients and health bionetwork might hamper the aspired progress of the Indian health care sector and health of the nation. With these rising costs and aging population, public leading a miserable life every day. Government need to take initiative of reexamining the health care system in some of the key features like assurance handling, compliance to treatment and care protocols, guidelines, cost control, disbursement models, integrity and technology enactment. In this situation, Wi-Fi transmission can be accessible with new traditions of health care delivery that lessens cost, diminishes victim's distress and man power. This wireless structure can be constructed using very large-scale integration (VLSI) concept which is appropriate for biogenic applications. VLSI design in biomedicine produces reduction in size of the chips, range, and speed enhancement. In this analysis, various proposals are scrutinized for VLSI employment of neural networks which is stated as CMOS fabrication technique, architecture of medical implant communication system (MICS) receiver for critical medical operations, field programmable gate array (FPGA) execution of semantic networks, neuro-fuzzy system, neuromorphic computing approach, neural net performance in analog hardware and digital network. Furthermore, the merits and demerits of these classifications and methods are covered here.**

***Keywords*:** Biomedical, Disbursement, FPGA, MICS, Neuromorphic, Protocol, VLSI**.**

I. Introduction

Today is the time of growth and on the other hand, it is also the period of growing pains. Moreover, the health care sector is restricted to three factors: allocation, utilization and awareness. Currently, there exists a big gap between these factors which leads to a disintegrated system with inadequate access to health care. Though the issues like enlarged aging trend, accessibility and privacy occur in medical care field but the evolution of technologies to solve health problems has developed fast so far. Here comes into the existence of wireless technology, which reduces the patient's pain points, cost and man power. Also, there are wireless devices available present day that are implanted in patients body with the accurate technology for monitoring patients and their medical conditions, the data access is very easy, cost is minimized and bed space is saved. Multi-objective optimization problem is the streamlining of various functions instantaneously and attaining a solution which is best in respect to all of the objective functions. These problems are present at various levels of VLSI circuit optimization [1]. Medical implant communication system (MICS) is a low power, short range (2 m), high data rate, (core band is 402-405 MHz) communication network which has been recognized across the globe for transferring the data to help the diagnostic or analeptic functions linked with medical implant devices [2], [3].

Neurology is the medical field worried with the detection and therapy of ailments of the nervous system, which includes the brain, the nerves and spinal cord. There are more than 600 diseases of the nervous systems, which include brain tumors, epilepsy, Parkinson's disease.

Artificial neural networks (ANNs) are computing systems virtually stimulated by the biological neurons that constitute animal brains. Such systems learn to accomplish task without being automated with particular rules. ANN uses the processing of brain as a valid point to build algorithms that can be used to guide complex patterns and prediction problems. ANN considers data samples rather than the entire data set for any solution which in turn save money and time. ANNs are networks of computing elements that have the capacity to respond to input stimuli and generate the desired output during

VLSI design of neural networks [4], [5]. Analog hardware needs to take care with respect to some key aspects: substrate-noise, variations in power supply, drift, leakage etc. But analog VLSI implementation of ANN by means of back propagation algorithm diminishes cost and power dissipation. In order to minimize the power consumption, analog feedforward neural networks are to be considered for solving the classification problems very easily [6], [7]. Digital neural networks are almost produced automatically from a logic description of their functions. Digital ones are well acquainted with new processes and hence redesigning is not required. With these new processes, power and area are lessened in order to make the digital circuits optimized [8], [9]. Digital neural networks are highly opted for classification problems even it is with or without analog-digital (AD) conversion of input signals. And moreover, digital networks surpass analog networks when it comes to with or without ADC [10].

The utilization of field programmable gate array (FPGA) for neural network design gives flexibility in programmable systems. With low precision neural network implementation, FPGAs have faster speed and lesser size for real time application than VLSI design [11], [12]. FPGA plays a very critical role in data sampling and processing industries due to its parallel architecture, low power consumption [13].The common neural network construction on FPGA SOC platform can achieve both forward and backward algorithms in deep neural networks (DNN) with high production and easily gets accommodated to the type and scale of the neural networks [14], [15]. FPGAs are some kind of hardware accelerators which provide programmable and huge parallel architecture. The mixture of power of GPUs with the reliability of FPGAs extends the scope of problems which can be accelerated [16].

Neuro-fuzzy systems are characterized as special multilayer feedforward neural networks. This system is educated by a learning algorithm derived from neural network theory. Fuzzy logic makes judgment on the basis of raw and uncertain data given to it. These are used to solve non-linear and complex problems [17], [18]. Fuzzy controller executes estimated reasoning on the basis of human way of perception to gain the control logic. De-fuzzifier alters the fuzzy output to the desired output in order to control the system [19].

In recent times, neuromorphic has been used to discuss about analog, digital, mixed-mode analog/digital VLSI and software systems that sketches the models of neural systems. The design of neuromorphic computing on the hardware level can be registered by oxide-based memristors, spintronic memories, threshold switches and transistors [20], [21]. Neuromorphic computing systems are highly connected and parallely consume relatively low power and process in memory [22]. Implementation of biomedical systems with the help of VLSI and wireless mechanisms are evolving day by day. Although the analog and digital types have their own advantages but while coming to design phase, digital ones are considered due to their robustness and ductility [23]. Spike sorting is the categorization in which, spike corresponds to which neuron and it is a very challenging problem. With the help of amplitude discriminator, separation of spike with respect to different neuron makes an easy way in terms of fastness and implementation time [24].

The paper is planned as follows. The literature review regarding VLSI implementation in biomedical applications is summarized in section 2. Comparison of previous works with the corresponding results is reported in section 3. Finally, section 4 concludes it.

II. Literature Review

Kashfi, F. et al. [1] reported multi-objective optimization method for VLSI circuits. This method successfully incorporates various forms of power and delay. In general, out of the two models: convex & non-convex, convex models achieve single step optimization based on an additional modelling error, while non-convex method peaks global optimum only if analytical gradient is used. Three methods: weighted sum, compromise programming (CP) and satisficing Trade-off method (STOM) help in achieving multi-objective optimization where analytical gradient and convex model results in good individual optimization. Weight sum is not preferred in resolution of multi-objective optimization issue. STOM is recommended based on the designer's interest in a certain point.

Kumar, V. S. B. et al. [25] studied on the current trends in VLSI design, which focuses on VLSI structures with bio-inspired algorithms. The testing results are based on assessing the performances levels of different VLSI studies in fixing the optimal precise values. Enhancements such as self-adaptive swarm optimization and VLSI optimal design are verified without the use of bio inspired algorithms. With utmost care, measure and analysis of floor planning issue is addressed.

Cassidy, S. A. et al. [20] provided an insight on neuromorphic architectures during the times of nano-CMOS; helps to understand the parallel communication connection responsibility for the build-up of spiking neurons and spike timing dependent plasticity (STDP) learning circuit. The neurons are thus treated as digital arithmetic logic units and communication processors, thereby paving the way to neural design optimization by spiking neurons & STDP learning, which help authentication of design methodology with potency of cortical growth.

Sonar, S. N., et al. [11] depicted the study of targeting area optimization in reconfigurable devices (FPGA) and it shows that area optimization as one of the major issues due to reconfigured structure for space applications. A new element Reed-Solomon (RS) encoder has been identified with the help of VHDL language, which takes very less area on FPGA but uses an ultra-low-cost VLSI planning of RS corrector. This RS corrector is associated with a solid hardware problem, addressed by utilizing the programmable resolution with respect to a mass variety of applications.

Hafliger, P. et al. [26] derived a single learning rule on the basis of Riccati equation that is used on volatile capacitive storage for synaptic weights. Moreover, time dependent learning rule is used to keep a track of temporal correlations in spike trains to get the estimated weight normalization.

Chen, A. C. et al. [27] planned for an active VLSI circuit design that consists of an adaptive fuzzy predictor, voting bases scheme and tri-stage entropy encoder, which helps in

increasing both proficiency and potency of electroencephalogram (EEG) signal transmission over wireless body area network (WBAN). Performance of compression rate is measured with an average value of 2.35 for 23 channels with the help of CHB-MIT Scalp EEG database, where the latest method delivered 14.6% upsurge in compression rate to 37.3% reduction is cost of the hardware. A pipelining technique has been used to expand the performance of the future design.

Chen, S.-L. et al. [28] preferred VLSI circuit design of micro control unit for WBSNs, consists of an asynchronous interface, a multi-sensor controller, a register bank, a hardware-shared filter, a lossless compressor, an encryption reader, an error correct coding (ECC) circuit, a universal asynchronous receiver/transmitter interface, a power management and a QRS complex detector. A hardware sharing procedure is utilized to diminish the silicon area of a hardware shared filter for outcome of low-pass, high-pass and band-pass filters with respect to several body signals, where the current encryption coder performs in increasing the average compression rate over 12% in ECG signal, providing body signal analysis and filtering security for WSBNs. In addition to that, QRS detector has been built to evaluate the ECG signals and encryption encoder on the basis of asymmetric cryptography process has been incorporated to safeguard the physical information throughout the data transmission.

Chen, S.-L. et al. [29] projected a lossless compression algorithm to minimize the transmission and storage data, where a look-up table framework helps to evaluate the performance and two-stage entropy encoder by using pipelining technology, thereby helping us to achieve lower hardware cost, minimal power consumption and a better compression rate with respect to other ECG encoder designs. Furthermore, VLSI architecture has been considered for wireless health care monitoring applications.

Chen, S.-L. et al. [30] defined hardware-oriented lossless method for ECG compression algorithm which is based on Huffman's coding in utilizing fuzzy decision and particle swarm optimizer (PSO) to gain high performance and low complexity, where the average compression rate is improved to 6.4% and condensed the gate count by a minimum of 8.2%. Here, it finds the optimal parameters by means of PSO algorithm to improve the accuracy of prediction values and the core area has been manufactured using a 90 nm CMOS fabrication procedure.

Mohana, M. S. et al. [31] approached to compress ECG in remote and zero lossless decompression by the use of a mixture of three different procedures: Strategic execution, Golomb rice coding and pressing configuration to expand the storage room by lessening the transmission time. Golomb rice coding has been utilized to encode the expectation error. Pressing configuration has been preferred to allow the constant interpretation process. The strategic execution is measured to make sure that it deploys more than 48 chronicles for MIT-BIH arrhythmia data set. This algorithm describes better finishing results when compared to previous lossless ECG compression process. Using Xilinx code, a decreased sophistication lossless external counter pulsation (ECP) pressure is achieved by a multi-purpose straight indicator setting versatile Golomb-rice.

Shalchyan, V. et al. [32] acquainted with wavelet-means manifestation which combines the wavelet shrinkage denoising along with multiscale edge detection for easy sensing and finding the occurrence of action potentials in noisy signals. An unsupervised optimization is offered to improve the uncovering performance by eradicating the dependency of the method with respect to mother wavelet. On the basis of correlation similarity measure another unsupervised criterion is explained to appraise the wavelet selection during clustering process to boost the spike sorting performance. The current method is compared with the past records with the help of wide range of accurate virtual data as well as certain trial recordings of intracortical signals from freely moving rats. The updating the wavelet selection of clustering process is shown to develop the classification performance in order to maintain the same wavelet as for the detection stage.

Lewicki, S. M. [33] reported the algorithms and methods for noticing and categorizing action potentials, possibly the major concern referred to as spike sorting. It confers the difficulties of neural activity and the common issues of signal sensing and classification. It studies and explains the algorithms and techniques applied to most of the problems in spike sorting and examine the pros and cons of each and the applicability of these methods for various types of experimental demands. It is written for the need of physiologist to use simple procedures which will enhance new yields and lower the selection preconceptions of old practices and also for those who are willing to spread on or encompass more cultured algorithms to meet new trial problems.

Rácz, M. et al. [24] aimed to present the current results on detection, classification and prediction of neural activities on the basis of multichannel action potential recordings. Deep learning models using convolution neural networks and a mixture of recurrent and convolution neural networks have been applied. Latter is used for spike detection and former one for sorting and anticipating spiking activities. An average accuracy of 89% in categorizing activities generated by more than 20 different neurons has been observed.

Elgendi, M. et al. [34] explained the lossy compression method III appropriate for remote health monitoring systems. This method is authorized with QRS detection and is reachable for smart homes, wearable devices and point-of-care systems. It provides the long-term and constant nursing for elderly and patients with inadequate agility and those with less access to health care. The specified substantial data collection, broadcast and scrutiny involved in monitoring process made method III to attain a compression ratio that is six times faster with a high QRS detection accuracy. The outcome proves the system readiness and usefulness of real time health care tracking.

Goldberg, H. D. et al. [35] presented a scheme for deploying the highly-linked; re-design networks of assimilate-and-fire neurons in VLSI. Neural activity is programmed by using spikes, whereas the report of an energetic neuron is connected through an unsynchronized request and acknowledgement cycle. Probabilistic transmission of spikes is selected to design synaptic weights and memory-based look-up tables to arrange arbitrary interconnection topologies. The construction is flexible, ascendable and well matched to multi-chip systems. Numerous modules are connected in series and parallel to

execute large-scale, multi-layered neural processing systems.

Crotty, P.et al. [36] investigated on the energy efficiency of inter spike interval neural codes. The hypothesis states that nature takes full advantage of information processing and its energy efficiency expanding the energy ratio based on the neuronal firing frequencies. Based on ISI and noise distributions, it is understood that anticipated ideal frequencies are in the same range and ISI codes are as effective as discrete binary and frequency codes.

Levy, W. B. et al. [37] announced the phrase "economy of impulses" to convey that the capability for consecutive neural systems makes use of lower and least levels of cell firings in order to produce an outcome of equal encodings. The final economy of impulses is a neural code of minimal idleness. To maintain the energy efficient information transmission, reduction in average firing rate is required which is achieved by both binary and analog neurons expenditure of neuron.

Murugan, S. et al. [12] talked about a receptive neural chip using FPGA as this helps in learning competence by manipulating the inherent parallelism of neural network. As a result, fast prototyping is conceivable for real-time applications, such as speech recognition, speech synthesis, image processing, pattern recognition and classification. On-chip learning method is manufactured to overcome XOR problem with the help of back propagation based multilayer perceptron and is applied in VIRTEX-E FPGA platform using VHDL code.

Hamdan, M. K. et al. [38] observed that convolution neural network (CNN) became popular with respect to accuracy and an effective algorithm, which has been used in various applications such as handwriting digit recognition, visual recognition and image classification. It is seen that a tool helps developers to automatically generate VHDL code over a configurable user-interface for their chosen CNN. This tool has been enhanced to create a flexible, accessible, reconfigurable and highly parallel implementation for CNN models. VHDL generator is described by applying a small-scale (Le-Net) and large-scale (Alex Net) CNN models on Virtex-7.

Meijer, B. L. P. [39] showcased that study of static feedforward neural network can help to contain continuous dynamic properties like delays and phase shift. It is representing a wide class of non-linear and dynamic systems, arbitrary nonlinear static and quasi-static as well as arbitrarily lumped linear dynamic systems where models' generators are executed for a range of pre-defined analog circuit simulators with support for VHDL-AMS and Verilog-AMS language standards.

Zhang, C. et al. [40] projected a roofline-model-based method for convolution neural network's FPGA acceleration. In addition to that, CNN for FPGA optimizes networks computation and memory access with the help of this model using enumeration and developed on Xilinx VC707 board which surpasses all earlier work. The best design for each layer is found out in this roofline model.

Shawahna, A. et al. [41] discussed the application of CNN in image detection and recognition. It focuses on acceleration techniques for deep learning algorithms from hardware point of view, based on the recent advancements of CNNs on FPGA. Key structures operated by various FPGA based CNN acceleration methods; helps gain precision and provide references in simulation. Efficient hardware is thus identified by use of tools for generating RTL scripts, which in turn helps in automating the design process and design space investigation.

Wang, T. et al. [16] systematically explored the neural network accelerator based on FPGA. A review on accelerator is carried out which is designed for particular algorithms, specific problems, algorithm features and general templates. Comparison is made on the design and implementation of the accelerator on the basis of FPGA under various devices and network models and also compared it with the CPU and GPU versions. The advantages and disadvantages of accelerators on FPGA platforms have been discussed to explore the operations research in future.

Guo, K. et al. [13] contemplated that CPU platforms faces difficulty in computational capacity whereas GPU overcomes the same. Further, the evaluation has been executed using various FPGA based accelerator designs with software and hardware methods to improvise the speed and energy efficiency. It is also said that neural networks are very well known for their great work in computer vision over traditional algorithms and are widely accepted in image, speech and video recognition. The state-of-the-art neural networks and the mechanisms used have been modified.

Ba ñuelos-Saucedo, M. A. et al. [8] focused on FPGA based digital implementation of McCulloch-Pitts neuron, consisting of non-linear activation function: step, ramp saturation and sigmoid helped to analyze the outcome based on speed and percentage of chip usage. The design of neurons is programmed via VHDL code and the simulation is done using Xilinx 3.0 software.

Dalgaty, T. et al. [21] attributed the stable development in computing systems for shrinking of semiconductor technology but, with severe physical and technological issues. A modern approach named neuromorphic computing accomplishes a physical image of a complete neuromorphic sensory-motor system by systematically processing the impression of how data flows through insectoids or animals. And as well, the neuromorphic computing as an evolving solution makes practice of silicon technology in various ways to detect the computational values.

Smith, L. S. [42] assisted by giving a modern view for both sensing and neural modelling producing systems using neuromorphic computational systems. The history and range of neuromorphic systems has been reviewed and executed respectively.

Upadhyay, N. K. et al. [22] studied that neuromorphic computing can learn and perform the task on its own by communicating with its surroundings. So, integrating that type of chip with CMOS processors will solve a variety of problems being faced by today's Artificial Intelligence (AI) systems. The basic operations like matrix multiplication and convolution depend on CMOS based multiply-accumulate units which are restricted by von Neumann bottleneck. Most of the emerging memory devices can perform vector matrix multiplication using Ohm's law and Kirchhoff's law. With the help of specific dynamics, these devices can be used as neurons or synapses in a neuromorphic computing system. It describes the emerging nano scale devices which can efficiently reconfigure the

computing paradigm in coming days.

Riyaz A. M. et al. [9] debated on complexity of human brain and faults of current available architecture, stressing on mixed mode operation of integrated circuits. Various software and hardware implementations to understand the modelling of neurons and morphed architectures are considered with explanation on software simulation and hardware emulation. As well, differences between FPGA and VLSI designs have been explained.

Moradi, S. et al. [43] helped in listing out the differences while working with CNN on-chip architectures and enabling existing methods for on-chip neuromorphic routing networks. Besides, it is mentioned that how memory and integration technologies help to ease the communication issues for the next generation intelligent computing machines.

Rajendran, B. et al. [44] worked on building of new class of human brain-inspired information processing engines that mimics the time-based data encoding and preprocessing aspect, defines the building blocks of neuromorphic computing utilizing Von Neumann computing styles. The ideas and specifications of building blocks of neuromorphic platforms, hardware neurons, synapses and architectures were defined to maintain the connectivity among them. Based on the nanoscale memristive devices, demonstration of certain calculations in place sidestepping the Von Neumann bottleneck and capturing timing-based correlation in signals is given. Likewise, some signal processing applications were discussed.

Qi, Y. et al. [14] suggested practical experiment with a multicore digital neuromorphic processing system helped compute image edge detection and ECG applications using FPGA with 3x and 127x speedup when compared to Intel processor design, with only a change in synaptic weight and number of neurons. Finally, these applications were developed with the help of Verilog code. The design and implementation have been carried out on Altera Quartus II FPGA platform.

Basu, A. et al. [45] discussed on updates to neuromorphic computing to support architectures and algorithms with on-chip learning, focusing on low-resolution synapses of standard algorithms with applications such as brain-machine interfaces, robotics and other future trends.

Rodr ́guez, F. G. et al. [15] worked on neuromorphic systems, implemented on FPGAs consist of framework boards connected to other platform such as SpiNNaker to allow successive events of spikes for boosting the motors, where neuro-inspired motor controller sends spike commands to robot post object detection and tracing for learning a task.

Lakha, S. B. et al. [17] approached the design of fuzzy logic controller for stepper motor is important due to the increase in demand for highly parallel and high-speed fuzzy processing linking hardware built of 2 inputs and 1 fuzzy logic controller. The implementation is done on Xilinx Spartan III with the help of VHDL coding.

Wilamowski, B. M. et al. [18] approached non-conventional structure for fuzzy controller to simplify microprocessor-based systems, doesn't require signal division though possessing same control surfaces as fuzzy controllers. The architecture of said process consists of fuzzification, MIN operators, normalization and weighted sum blocks with 2 um n-well technology.

Sadati, N. et al. [19] corresponded to the notion that the neuro-fuzzy controller can be utilized for a huge variety of processes. In this case, the inputs signals, output signals and processing circuits are analog whereas the chip is programmed digitally. And analog ones allow design of effective circuits in terms of low power, fast and dense. The anticipated approach for high speed and supple defuzzification utilizes various methods using a 3-layer neural network: center of gravity, mean of maxima eradicating the need for division thereby removing the speed bottlenecks of the preceding works.

Bosque, G. et al. [46] differentiated work of over last two decades and the beginning of present decade relevant to hardware classification. Thus, it is highlighted the characteristics of hardware implementations of fuzzy systems, neuro-fuzzy systems and neural networks.

Zhang, D. et al. [47] accentuated the management between fully convolutional networks (FCN) definition, description and systolic implementation. It offers elasticity, programmability and correctness with high throughput and local interconnections.

Shrinath, A. K. [4] worked on anticipated neural network plan, which is used for analog operations like amplification and frequency multiplication using analog components such as: Gilbert cell multiplier, adders and activation functions. The architecture is accomplished using back propagation with new methods of weight storage. And for scheming and authentication purpose, 45 nm CMOS technology is preferred. The proposed neural network is used for analog operations like amplification and frequency multiplication.

Pasero, E. et al. [5] delivered the silicon implementation of a basic cell for artificial neural systems that uses analog techniques to design the computing kernel. The network has an in-built learning capability which executes the discrete delta rule. A prototype chip is under construction whose performance has been customized to typical pattern recognition applications.

Song, L. Y. et al. [6] established that the advantage of an artificial neural network algorithm completely is based on the hardware on which it is to be executed. Based on the similar circuit configuration for neural & electronic systems, it is easier to implement many neural functions in VLSI. Due to low-precision processing, analog devices take over digital ones. Similarly, ANNs are found to be resistant of lesser-precision elements to conventions systems based on common components such as adders, multipliers which are silicon area efficient on a comparative basis in the applications for minimal precision.

Hurdle, J. F. et al. [48] debated that synchronous VLSI design as extremely important. Clocked circuits have every valuable piece of electronic hardware usage in this era. Additionally, these are supported by large and functional set of computer-aided design (CAD) tools from high level recognition to robotic fusion systems to have placement and routing benefits. Though the synchronous design has its own power and potentiality, but here in this case asynchronous systems are chosen as it matches neurocomputing in a general and stabilized way. Generally, it has been claimed that asynchronous patterns hold great capacitance in resolving spiky design issues faced by neural hardware researchers such

as: scaling of neural circuits, composing neural units, circuit strength and process resistant performance.

Mazumdar, S. M., [49] demonstrated a possible normal training approach for feedforward type neural networks in view of VLSI design. The gradient sequence based back propagation model is lessened to evaluate the stochastic type of neural hardware. Furthermore, this learning algorithm is only used for add, subtract and logical operations to minimize the circuit complexity with speed improvement. The forward and reverse characteristics on perceptron's have been executed by means of casual threshold logic. The hardware which has been advised contains 31 perceptron's per sheet and works in parallel manner with a programmable number of layers running in sequential mode.

Graf, H. P. et al. [7] opted for building an electronic neural network (ENN) memory with 256 neurons on a single chip using analog and digital VLSI technology and also by means of convention fabrication mechanism. In order to make the inhibitory connections and simulations for neurons, amplifiers with inverting and non-inverting outputs have been taken into consideration. The relation between specific neurons is contributed by amorphous-silicon resistors which are placed on a CMOS chip as part of last step in production phase. This method gives a very solid filling of the neurons. Electron-beam direct-writing has been used to guide the resistors to change the data stored in the network from one chip to next very efficiently.

Im, J. et al. [50] has proposed an effective scheme and VLSI architecture of a high data rate medical implant communication systems (MICS) digital base-band transmitter for implantable medical devices. An orthogonal frequency division multiplexing (OFDM) relevant multicarrier system has been introduced to solve the data rate problem occurred by narrow bandwidth of 300 kHz. The transmitter which has been thought off offers improvised data rate by combining multiple channels at same time. In addition to that, for getting proper MICS regulation, various schemes have been applied by including optimized subcarrier proportion for inverse fast Fourier transform (IFFT) and secured side lobe suppression technique. The transmitter which has been approached with better hardware plan has been built by VLSI implementation and also supports a maximal data rate of 4.86 Mbps which is ten times faster than the precedent systems.

Venkateswari, R. et al. [2] came up with a new feature called cyborg which controls the robotic arm with the help of brain implant. The architecture of implantable node has become popular as the surgically rooted node intakes very less power. Additionally, an effective CMOS transmitter with reference to low-power has been considered for implantable medical devices in the MICS band range. The architecture has been accomplished by means of cadence RF spectre tools along with 180 nm methodology and thus transmitter front-end consumed 900 microwatt power for the respective MICS receiver band.

Islam, M. N. et al. [3] noticed that medical implant communication system is a low-power, short range and high data rate transmission network which has been accepted globally for broadening data in order to look after diagnostic or therapy functions linked with medical implant devices. The progress of MICS devices has been well-focused and the technical points for successful MICS design has been defined with respect to the references declared by several frequency management's authorities across the world.

Tekin, A., et al. [51] stated regarding the new un-licensed band offering 402-405 MHz frequency which has been allocated to medical communication systems (MICS) provided regulations by Federal Communication Commission (FCC) and hence used by the transceiver. Even though this band produces low body absorption characteristic at these frequencies but it causes many threats to RF designers. The investigation has been done on the construction of a fully integrated 402 MHz, 0.18 um low power CMOS transmitter. Some of the issues associated with full integration have been discussed. Both the system and circuit level problems have been described here.

Chiueh, D. T. et al. [52] communicated with reference to the VLSI design and testing of a high capacity associative memory called as exponential correlation associative memory (ECAM). It has been noted that the sample 3 micro-CMOS programmable chip is efficient of storing 32 memory patterns for each 24 bits. The work of ECAM chip has been showed as good as computer-virtual ECAM. This chip gives a fast and better way of response for solving many coherent issues like vector quantization and optical character recognition.

Venkatesh, S. et al. [10] focused on analog design of hybrid multiplier architecture where current is multiplied with the digital weights. The multiplier has three sub-components which are as follows: DAC, current steering circuits and a current mirror circuit. The fabrication and validation of Synapse has been done using cadence virtuoso. The accuracy and power of the circuit is checked to get better performance. The service has been verified by using AvanWaves. The architecture which was predicted followed R-beta R model for digital to analog conversion. The layout for MDAC, RC extraction and GDSII for MDAC has been studied.

III. Results and Comparison

In this section, earlier performances with respect to neural networks are explored and equated. The different attributes related to the proportional works are also demonstrated with the application of several technologies. The concerns and achievements of respective works are also observed. Here, different works are tabulated based on biomedical applications through the implementation of VLSI.

Table 1 shows the analogy of various VLSI implementations based on neural networks systems. Ultimately, a fully integrated neural network with less cost, minimum power and moderate area by adopting VLSI and wireless mechanism is aimed for the future work.

Refs.	Parameters	Implementation Type	Issues	Output	Tools / Technology Used
[1]	Power, delay	Multi objective method	Weighted Sum: Less effective for solving multi-objective optimizations problems	Power dissipation, delay	VLSI
[25]	Power consumption, size, quality	Self-adaptive particle swarm optimization	Different designs of VLSI	NA	VLSI
[20]	Energy, delay, costs	FPGA	Physical size constraint	Design of spiking neurons and STDP learning circuits	Nano silicon and nano CMOS technology
[11]	Forward error correction	FPGA	Area optimization	Low cost VLSI architecture for RS corrector	VHDL
[26]	Action-potential neurons	Riccati equation learning rule	Large connectivity	Weight normalization, temporal correlations	VLSI
[27]	Compression rate	Lossless compression algorithm, pipelining technique	Power consumption	Lossless EEG compression circuit with increased compression rate and lesser hardware cost	VLSI
[28]	Chip area, cost and compression rate	Asymmetric encryption method	Privacy of the information and power consumption	Increased compression rate in ECG signal and best security for wireless body sensor networks	VLSI
[29]	Cost, power consumption	Pipelining technique and two-stage entropy encoder	NA	Low power, lesser cost and good compression rate ECG encoder design for wireless health care monitoring	VLSI

[30]	Gate count, compression rate	Fuzzy based particle swarm optimizer and Huffman entropy coding techniques	NA	Improved compression rate and reduced gate count ECG design for wearable devices	VLSI
[31]	Pressure rate, window size	FPGA	Heart issues for portable cases	Good ECG pressure calculation	Xilinx programming
[32]	Spike detection and sorting	Unsupervised optimization method	Issues with the choice of mother wavelet shape, colored noise	Upgraded detection and classification performance	Brain computer interfacing
[33]	Action potentials, spike sorting	Bayesian clustering and classification method	Time consuming, robustness	Good action potentials with spike shape and spike timing	Computer technology
[34]	Compression rate, QRS detection accuracy	Lossy compression Method III	NA	High QRS detection accuracy for health care monitoring	Embedded and mobile technology
[35]	Neurons, synaptic weights	Probabilistic synaptic weighting	Modelling issues	Good computations in address domain and spike timing	Analog VLSI, MATLAB
[36]	Energy ratio	Hypothesis method	NA	Efficient noise levels	Information processing
[37]	Binary and analog neurons	Optimization and neuronal coding approach	NA	Increase in energy expenditure per neurons	Information processing and energy efficient transmission
[12]	Neural chip	Virtex-E FPGA, On-chip learning method	XOR problem	Speech recognition, image processing and classification	VHDL
[38]	VHDL generation tool	FPGA, optimization method	NA	Image processing and peak performance	VHDL, Xilinx Virtex-7
[39]	Delay, phase shift	Hybrid modelling approach	NA	Dynamic neural networks	Verilog-AMS
[40]	CNN acceleration	Loop tiling and transformation method	Complexity and scalability	Peak performance	Convolution neural networks technique

[41]	Acceleration performance	FPGA	NA	Implementation of deep learning networks	Artificial intelligence, deep learning
[13]	Speed, energy efficiency	FPGA	Pattern recognition problems	10 times better speed and energy efficiency	Neural network, parallel processing
[8]	Operation speed	FPGA	Performance issues	Implementation of powerful ANN	VHDL
[21]	Insect-inspired nervous systems	Neuromorphic computing, central pattern generators	Classification problems	Low-power computing systems, chemical sensing, sound processing and motor system control	VLSI, silicon technology
[42]	Synapses, complexity	Event bus technique, CMOS	Long delay, interconnectivity, adaptiveness	Effective adaptive synapses in big number	VLSI
[9]	Brain modelling, synapses, neural networks	FPGA, CMOS	Learning and memory issues, some research issues related to software and hardware implementations	NA	VLSI, Xilinx
[43]	Power, routing memory, bandwidth	FPGA and CMOS	Reliability, scalability, static power issues, integration issues	Implementation of large-scale neuromorphic designs with respect to power and bandwidth	VLSI
[44]	Energy efficiency, synapses, spiking neurons	Pragmatic hardware implementation and spiking network type, FPGA	Time, ambient temperature, reliability and variability	Construction of energy efficient neuromorphic computing platforms	CMOS
[14]	Edge detection and ECG	FPGA	NA	Virtuous speedup-for edge detection and ECG applications	VHDL
[45]	Weight, power, synapses and energy	CMOS, feedback alignment method	Selectivity issues	Adaptive neuromorphic systems	Random backpropagation, spintronic technology
[15]	Spike-based commands	FPGA, ED-Scorbot framework	NA	Spike-based neuromorphic system	VHDL, robotic technology
[17]	Speed, performance	FPGA	NA	Design of fuzzy logic controller	Xilinx Sparten III, VHDL
[18]	Weight,	Fuzzification,	Stability	Non-convention	VLSI, 2um

	accuracy	normalization and weighted sum, Takagi- Sugeno approach		al structure for a fuzzy controller	n-well technology
[19]	Speed, fuzzy rules	CMOS, neuro fuzzy approach, defuzzification	NA	Analog neuro-fuzzy controller	VLSI, neural networks
[46]	Images, neurons, speed, performance	FPGA	Data representation, update of weights, nature of learning algorithm, design constraints and general issues-sigmoid and ramp	Development of fuzzy systems, neural networks and neuro-fuzzy systems	VLSI, CMOS technology, bipolar device technology, Xilinx
[47]	Throughput, local interconnectio ns	System design methodology	Performance issues	Fuzzy clustering neural network model	VLSI
[4]	Neural networks, weight storage	Analog type	System level issues	Implementation of feed forward neural network for analog signal processing	CMOS VLSI technology
[5]	Kernel, prototype chip	Analog type	NA	Model of a basic cell for Artificial Neural Systems	VLSI
[6]	Precision	Circuit implementation, analog type	NA	Efficient Artificial Neural Network with lesser precision	VLSI
[48]	Scaling, tolerance, performance	FPGA	NA	Implementation of Neural System	Asynchronous VLSI
[49]	Complexity, speed	Back propagation technique, stochastic algorithm	NA	Architecture of Multi-layer feed forward neural network	VLSI
[7]	Neurons	CMOS fabrication process	NA	Construction of Electronic Neural Network	Analog and Digital VLSI with micro fabrication process
[50]	Data rate	Orthogonal frequency division multiplexing, inverse fast Fourier-transform and side lobe suppression method	NA	Development of a high data rate Medical Implant Communication System	VLSI
[2]	Power	RF-front end transmitter, body sensor network	Complexity of human body, safety concerns and some technological bottlenecks	MICS band Low Power Transmitter for Medical Implantable Devices	Cadence RF Spectre tools, 180nm CMOS technology

[3]	Power, data rate	MAC protocol, telemetry	Network issues	MICS network implementation	Communicatio n networks and body sensor networks
[51]	Frequency band, power	FSK transceiver, ring VCO with direct modulation	System and circuit level issues	Low-Power MICS-transceiv er architecture	CMOS
[52]	Performance, capacity correlation	MOS transistors, correlation based associative memories	NA	High capacity neural network	VLSI
[10]	Weight, accuracy, power	MDAC architecture, analog type	Gain error	Novel hybrid neural network multiplier architecture	Analog VLSI

Table 1. Comparison of various VLSI implementation based neural network systems

IV. Conclusion

The integrated neural network operating VLSI design with low cost, low power and low area are highly necessary in biomedical systems. MICS receiver with improved RF circuitry is crucial building blocks for auditing, investigation and control functions in biogenic appliances. The additional techniques of VLSI design include FPGA implementation, neuromorphic computing and neuro-fuzzy approach, which are demanding in the biomedical application. FPGA performs parallel processing with a faster rate. Neuromorphic computing has the key feature of good durability. Neuro-fuzzy systems are useful for most of the practical medical applications. The literature survey and observation table will help the analyst for further groundwork in this domain.

References

[1] F. Kashfi, S. Hatami, M. Pedram. *Multi-Objective Optimization Techniques for VLSI Circuits*, University of Southern California, Los Angeles, CA, 2011.

[2] R. Venkateswari, R. S. Subha. "Design of MICS Band Low Power Transmitter for Implantable Medical Applications", *Advanced Materials Research*, pp. 1223-1228, 2014.

[3] M. N. Islam, M. R. Yuceb. "Review of Medical Implant Communication System (MICS) band and network*", ICT Express*, 2, pp. 188-194, 2016.

[4] A. K. Shrinath. "Analog VLSI Implementation of Neural Network Architecture", *International Journal of Science and Research*, pp. 2319-7064, 2013.

[5] E. Pasero, L. M. Reyneri. "An Analog Cell for VLSI Implementation of Neural Networks", *Neurocomputing*, 68, pp. 153-156, 1990.

[6] L. Y. Song, Vannelli, M. I. Elmasry. "A Compact VLSI Implementation of Neural Networks", *VLSI Artificial Neural Networks Engineering*, pp. 139-156, 1994.

[7] H. P. Graf, L. D. Jackel, R. E. Howard, et al. "VLSI implementation of a neural network memory with several hundreds of neurons", In *AIP Conference Proceedings*, 151(1), pp. 182, 2008.

[8] M. A. Bañuelos-Saucedo, J. Castillo-Hernández, S. Quintana-Thierry, et al. "Implementation of A Neuron Model using FPGAs", *Journal of Applied Research and Technology*, 1(3), pp. 248-253, 2003.

[9] A. M. Riyaz, B. K. Sujatha. "A Review on Methods, Issues and Challenges in Neuromorphic Engineering", *International Conference on Communication and Signal Processing*, pp. 2-4, 2015.

[10] S. Venkatesh, P. C. Prasanna Raj. "Analog VLSI Implementation of Novel Hybrid Neural Network Architecture", In *Proceedings Analog VI*, 7(2), pp. 62-66, 2008.

[11] S. N. Sonar, R. R. Mudholkar. "ECC design strategy targeting area optimization in reconfigurable device (FPGA) using VLSI technique", *International Journal of Engineering Studies*, 9 (1), pp. 1-9, 2017.

[12] S. Murugan, K. P. Lakshmi, J. Sundar, et al. "Design and Implementation of Multilayer Perceptron with On-chip Learning in Virtex-E", In *2nd AASRI Conference on Computational Intelligence and Bioinformatics*, pp. 82-88, 2014.

[13] K. Guo, S. Zeng, J. Yu, et al. "A Survey of FPGA Based Neural Network Accelerator", *ACM Transactions on Reconfigurable Technology and Systems*, 9(4), pp. 1-26, 2017.

[14] Y. Qi, B. Zhang, T. M. Taha, et al. "FPGA Design of a Multicore Neuromorphic Processing System", In *IEEE National Aerospace and Electronics Conference*, pp. 255-258, Dayton, USA, 2014.

[15] F. G. Rodríguez, A. Jiménez-Fernández, F. Pérez-Peña, et al. "ED-Scorbot: A Robotic test-bed Framework for FPGA-based Neuromorphic systems", In *6th IEEE International Conference on Biomedical Robotics and Bio-mechatronics (Bio-Rob)*, pp. 237-242, Singapore, 2016.

[16] T. Wang, C. Wang, X. Zhou, et al. "An Overview of FPGA Based Deep Learning Accelerators: Challenges and Opportunities", In *IEEE 21st International Conference on High Performance Computing and Communications; IEEE 17th International Conference on Smart City; IEEE 5th International Conference on*

Data Science and Systems (HPCC/SmartCity/DSS), pp. 1674-1681, China, 2019.

[17] S. B. Lakha, R. Goyal, R. Kumar, et al. "Design and VLSI implementation of Fuzzy Logic Controller", *International Journal of Computer and Network Security*, 1(3), pp. 1-5, 2009.

[18] B. M. Wilamowski, R. C. Jaeger. "VLSI Implementation of A Universal Fuzzy Controller", *IEEE Transactions on Industrial Electronics*, 46(6), pp. 1132-1136, 2000.

[19] N. Sadati, H. Mohseni. "A VLSI Neuro-Fuzzy Controller", *Intelligent Automation and Soft Computing*, 5(3), pp. 239-255, 2013.

[20] S. A. Cassidy, J. Georgiou, A. G. Andreoua. "Design of silicon brains in the nano-CMOS era: Spiking neurons learning synapses and neural architecture optimization", *Neural Networks*, 45, pp. 4-26, 2013.

[21] T. Dalgaty, E. Vianello, B. De Salvo, et al. " Insect-inspired neuromorphic computing", *Insect Science*, 1, pp. 59-66, 2018.

[22] N. K. Upadhyay, H. Jiang, Z. Wang, et al. "Emerging Memory Devices for Neuromorphic Computing", *Neuromorphic Computing*, 4(4), pp. 1-13, 2019.

[23] N. Sowmya, S. S. Rout,. "A Review on VLSI Implementation in Biomedical Application", In *10th International Conference on Innovations in Bio-Inspired Computing and Applications*, Gunupur, India, 2019. (In Press)

[24] M. Rácz, C. Liber, E. Németh, et al. "Spike detection and sorting with deep learning", *Journal of Neural Engineering*, 17(1), pp. 1-30, 2020.

[25] V. S. B. Kumar, P. V. Rao, H. A. Sharath, et al. "Review on VLSI design using optimization and self-adaptive particle swarm optimization", *Journal of King Saud University-Computer and Information Sciences*, pp. 1-12, 2018.

[26] P. Hafliger, M. Mahowald, L. Watts. "A spike-based learning neuron in analog VLSI*", Advances in Neural Information Processing Systems*, pp. 692-698, 1996.

[27] A. C. Chen, C. Wu, R. A. P. Abu, et al. "VLSI Implementation of an Efficient Lossless EEG Compression Design for Wireless Body Area Network", *Applied Sciences*, 8(9), pp. 1474, 2018.

[28] S.-L. Chen, C. M. Tuan, Y. H. LEE, et al. "VLSI Implementation of a Cost-Efficient Micro Control Unit with an Asymmetric Encryption for Wireless Body Sensor Networks", *IEEE Access*, pp. 4077-4086, 2017.

[29] S.-L. Chen, J.-G. Wang. "VLSI implementation of low-power cost-efficient lossless ECG encoder design for wireless healthcare monitoring application", *Electronics Letters*, 49 (2), pp. 91-93, 2013.

[30] S.-L. Chen, C. M. Tuan, T. K. Chi, et al. "VLSI architecture of lossless ECG compression design based on fuzzy decision and optimisation method for wearable devices", *Electronics Letters*, 51(18), pp. 1409-1411, 2015.

[31] M. S. Mohana, S. Jayachitra. "An Efficient Code Compression Technique for ECG Signal Application using Xilinx Software", *International Journal of Scientific & Technology Research*, 8(9), pp. 1958-1965, 2019.

[32] V. Shalchyan, D. Farina. "Spike Detection and Clustering with Unsupervised Wavelet Optimization in Extracellular Neural Recordings*", IEEE Transactions on Biomedical Engineering*, 59(9), pp. 2576-2585, 2012.

[33] S. M. Lewicki. "A review of methods for spike sorting: the detection and classification of neural action potentials", *Network: Comput. Neural Syst.*, 9, pp. 53-78, 1998.

[34] M. Elgendi, A. Al-Ali, A. Mohamed, et al. "Improving Remote Health Monitoring: A Low-Complexity ECG Compression Approach", *Diagnostics (Basel)*, 8(1), pp. 1-17, 2018.

[35] H. D. Goldberg, G. Cauwenberghs, G. A. Andreou. "Probabilistic synaptic weighting in a reconfigurable network of VLSI integrate-and-fire neurons", *Neural Networks*, pp. 781-793, 2001.

[36] P. Crotty, W. B. Levy. "Energy-efficient interspike interval codes", *Neurocomputing*, 65, pp. 371-378, 2005.

[37] W. B. Levy, R. A. Baxter. "Energy Efficient Neural Codes", *Neural Computation*, 8(3), pp. 531-543, 1996.

[38] M. K. Hamdan, D. T. Rover. "VHDL Generator for A High Performance Convolutional Neural Network FPGA-Based Accelerator", In *International Conference on Reconfigurable Computing and FPGAs*, pp. 1-6, Cancun, Mexico, 2017.

[39] B. L. P. Meijer. "Neural Networks for Device and Circuit Modelling", In *Conference Scientific Computing in Electrical Engineering*, pp. 251-258, Warnemünde, Germany, 2000.

[40] C. Zhang, P. Li, G. Sun, et al. "Optimizing FPGA-based Accelerator Design for Deep Convolutional Neural Networks", In *Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, pp. 161-170, 2015.

[41] A. Shawahna,, S. M. Sait, A. El-Maleh. "FPGA-based Accelerators of Deep Learning Networks for Learning and Classification: A Review Neural and Evolutionary Computing", *IEEE Access*, pp. 7823-7859, 2018.

[42] L. S. Smith. "Neuromorphic Systems: past, present and future", *Advances in experimental medicine and biology*, pp. 167-182, 2010.

[43] S. Moradi, R. Manohar. "The Impact of On-chip Communication on Memory Technologies for Neuromorphic Systems", *Journal of Physics D: Applied Physics*, 52(1), pp. 1-11, 2019.

[44] B. Rajendran, A. Sebastian, M. Schmuker, et al. "Low-Power Neuromorphic Hardware for Signal Processing Applications: A Review of Architectural and System-Level Design Approaches", *IEEE Signal Processing Magazine*, 36(6), pp. 97-110, 2019.

[45] A. Basu, J. Acharya, T. Karnik, et al. "Low-Power, Adaptive Neuromorphic Systems: Recent Progress and Future Directions", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 8(1), pp. 6-27, 2018.

[46] G. Bosque, I. Del Campo, J. Echanobe. "Fuzzy systems, neural networks and neuro-fuzzy systems: A vision on their hardware implementation and platforms over two decades", *Engineering Applications of Artificial Intelligence*, 32, pp. 283-33, 2014.

[47] D. Zhang, S. K. Pal. "A Fuzzy Clustering Neural Networks (FCNs) System Design Methodology", *IEEE Transactions on Neural Networks*, 11(5), pp. 1174-1177, 2000.

[48] J. F. Hurdle, E. L. Brunvand, L. Josephson. "Asynchronous VLSI Design for Neural System Implementation", *VLSI for Neural Networks and Artificial Intelligence*, pp. 129-139, 199.
[49] S. M. Mazumdar. "A multilayered feed forward neural network suitable for VLSI implementation", *Microprocessors and Microsystems*, 19(4), pp. 231-234, 1995.
[50] J. Im, Y. Jung, S. Lee, et al. "High-speed multicarrier transmission scheme for implantable medical devices", *IEICE Electronics Express*, 8(3), pp. 143-148, 2011.
[51] A. Tekin, M. R. Yuce, W. Liu. "A Low Power MICS Band Transceiver Architecture for Implantable Devices", *IEEE Annual Conference Wireless and Microwave Technology*, FL, USA, 2005.
[52] D. T. Chiueh, M. R. Goodman. "VLSI Implementation of a High-Capacity Neural Network Associative Memory", In*: Advances in Neural Information Processing Systems 2*, pp. 793-800, San Mateo, CA, 1990.

Author Biographies

Nagavarapu Sowmya completed her M.Tech in Electronics and Communications Engineering from Gandhi Institute of Engineering and Technology University, Gunupur, India in 2019. Currently, she is continuing her Ph.D. at GIET University, Gunupur, India. Her research areas are VLSI design, Biomedical, Neural networks.

Shasanka Sekhar Rout completed his Ph.D. at VSS University of Technology (VSSUT), Burla, India in 2019. He received his M.Tech degree in VLSI signal processing from VSSUT, Burla, India in 2014. He is currently working as Assistant Professor in GIET University, Gunupur, India. He has more than 20 publications in his research domain. His research area focuses on VLSI signal processing, analog and RF CMOS circuit design, digital VLSI design.

Rajesh Kumar Patjoshi completed his Ph.D. at National Institute of Technology (NIT), Rourkela, India in 2015. He received his M.Tech degree in VLSI and embedded systems from NIT, Rourkela, India in 2010. He is currently working as Associate Professor in NIST, Berhampur, India. He has more than 25 publications in his research domain. His research interest includes power quality enhancement, analog and mixed signal VLSI design and grid integrated of renewable energy network control.