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Article

Voltage-Aware Optimization of a 16-Transistor Radiation-Hardened SRAM Cell for Low-Power and Reliable Operation in 16 nm CMOS Technology

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Abstract: Aggressive scaling of CMOS technology into the 16 nm regime has intensified the long-standing conflict between low-power operation and radiation robustness in embedded Static Random Access Memory (SRAM), particularly for aerospace, defense, and deep-space electronics in which soft errors such as single-event upsets (SEUs) threaten data integrity. While numerous radiation-hardening-by-design (RHBD) topologies have been proposed to mitigate such errors, the majority rely on increasing transistor count or layout redundancy, which inflates area and power overhead without directly addressing the underlying trade-off among critical charge (Qcrit), static noise margin (SNM), leakage current, and delay. This work develops a voltage-aware optimization framework for a proposed 16-transistor (16T) radiation-hardened SRAM cell, implemented using 16 nm CMOS Predictive Technology Model (PTM) transistors within the HSPICE simulation environment. The cell integrates redundant storage nodes, decoupled read/write access paths, and dedicated upset-recovery transistors to suppress single- and multi-node upsets. Supply voltage was swept from 0.5 V to 1.0 V, and read delay, write delay, leakage current, SNM, Qcrit, and power-delay product (PDP) were extracted to characterize the cell across its operating range. Results show that leakage current and PDP rise sharply beyond 0.8 V due to intensified subthreshold conduction, whereas SNM and Qcrit increase monotonically with VDD, confirming improved radiation hardness at higher supply levels. The moderate-voltage region (0.6-0.8 V) is identified as the optimal operating band, balancing speed, leakage, stability, and radiation tolerance without increasing transistor count or circuit area. These findings provide practical guidance for voltage-aware SRAM design in radiation-prone, energy-constrained nanoscale CMOS systems, with future work targeting layout-level, parasitic-aware, and experimental irradiation validation of the proposed architecture.
Keywords: SRAM; 16 nm CMOS; Radiation Hardening; Low-Power Design; Static Noise Margin; Critical Charge; Power-Delay Product; HSPICE

1. Introduction

1.1 Background and Motivation

Static Random Access Memory (SRAM) remains one of the most critical building blocks of modern digital systems, providing low-latency, high-bandwidth storage for processor caches, register files, and embedded memory arrays. As CMOS technology continues its migration into deep-submicron and nanoscale nodes such as 16 nm, SRAM design is increasingly constrained by a combination of power dissipation, stability, process variability, and reliability challenges (Kumar & Mukherjee, 2023). The conventional six-transistor (6T) cell, long favored for its compact area,


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suffers pronounced degradation at these dimensions: short-channel effects erode threshold-voltage control, subthreshold and gate leakage currents grow as oxide thickness scales down, and random dopant fluctuation together with line-edge roughness introduce mismatch that directly narrows the static noise margin (SNM) and write margin of the cell.

As device dimensions shrink further, power consumption becomes the dominant design concern, particularly for battery-powered and energy-constrained platforms such as Internet-of-Things (IoT) nodes, mobile system-on-chip processors, and edge-computing accelerators, all of which depend heavily on on-chip SRAM for data storage and retrieval. To address this, the research community has pursued several complementary directions, including multi-transistor cell architectures (8T, 9T, 10T, and beyond), aggressive supply-voltage scaling, and assist circuits such as negative bit-line, boosted word-line, and adaptive body-biasing schemes. Each of these approaches improves one axis of performance, typically at the expense of another, which motivates a more systematic, trade-off-aware approach to SRAM design rather than isolated circuit-level fixes.

In parallel with the power challenge, reliability concerns have become equally pressing. SRAM cells fabricated in advanced nodes such as 16 nm exhibit heightened sensitivity to external disturbances, including radiation-induced soft errors, process variation, and electrical noise. These effects can corrupt stored data, degrade manufacturing yield, and in the worst case cause system-level failure -- consequences that are unacceptable in aerospace, satellite, automotive, and other safety- or mission-critical applications where the cost of a single undetected bit-flip can be severe.

1.2 Radiation Effects and Reliability Challenges in SRAM

Radiation-induced failures, principally Single Event Upsets (SEUs) and Single Event Transients (SETs), are of growing concern as SRAM design enters the nanoscale regime (Lim & Jo, 2025). These effects occur when a high-energy charged particle -- originating from cosmic rays, trapped-belt protons, or terrestrial alpha and neutron sources -- strikes a sensitive circuit node and deposits a transient charge sufficient to flip the stored logic state. Because the critical charge (Qcrit) required to upset a node scales down together with transistor dimensions and supply voltage, nanoscale SRAM cells are intrinsically more vulnerable to such events than their planar predecessors, and a single particle strike can increasingly disturb more than one node simultaneously, giving rise to multi-node upsets (MNUs) that defeat simple single-bit error-correction schemes.

Conventional 6T and 8T SRAM cells offer little inherent resilience to SEUs or SETs, since their storage nodes are closely spaced and lack redundancy. To address this, the community has developed a family of Radiation-Hardening-by-Design (RHBD) architectures -- including DICE, Quatro, and related multiple-upset-tolerant topologies -- that improve resiliency through redundant storage nodes, cross-feedback restoration paths, or decoupled sensing. More recently, 12T, 13T, 14T, and 16T hybrid radiation-hardened cells have been proposed specifically to withstand multi-node upsets, offering substantially higher critical charge and read/write stability relative to classical 6T and 8T designs, generally with only a modest increase in power (Kim & Jo, 2025). Sixteen-transistor architectures, in particular, tend to separate read and write access paths entirely, which both improves radiation resilience and removes read-disturb failure modes that otherwise limit SNM in denser cells.

1.3 Low-Power Design Considerations in 16 nm CMOS

Power reduction strategies for SRAM are generally categorized as dynamic-power reduction and leakage-power reduction. Dynamic power arises primarily from the repeated charging and discharging of bit-lines and word-lines during read and write operations, while leakage power originates from subthreshold conduction and gate-tunneling current, both of which intensify as device dimensions and gate-oxide thickness are scaled down (Yekula et al., 2022). In 16 nm CMOS technology specifically, leakage power grows disproportionately as supply voltage and oxide thickness are reduced, which has motivated a range of mitigation techniques including subthreshold and near-threshold operation, voltage scaling, reduced bit-line swing, and energy-recycling circuit techniques. Complementary layout-

level strategies -- such as stacking transistors to lengthen the effective leakage path and decoupling read circuitry from the storage core -- further reduce standby power without requiring aggressive voltage reduction (Dwivedi et al., 2024).

Advanced SRAM topologies, including 10T and 16T cells, provide improved trade-offs between power and performance by separating read and write operations (Fuad & Nayan, 2026; Bhatta et al., 2024). This separation reduces unnecessary internal node switching and improves noise immunity during reads, since the storage nodes are no longer directly loaded by the sensing bit-lines. Differential 10T cells, for example, have been reported to achieve markedly higher static margins than 6T designs while simultaneously reducing power consumption (Jarollahi & Hobson, 2013), illustrating that architectural decoupling -- rather than transistor count alone -- is often the more effective lever for jointly improving stability and efficiency.

1.4 Trade-offs between Power, Stability, and Radiation Robustness

Designing SRAM cells in 16 nm CMOS technology is inherently a multi-objective problem involving power, area, speed, and reliability, all of which interact non-linearly (Islam et al., 2020). Increasing transistor count from 6T toward 12T, 14T, or 16T architectures generally improves radiation robustness through added redundancy (Aiello et al.), but simultaneously increases layout area and, in many implementations, complicates low-power operation. Balancing these competing requirements while maintaining manufacturability remains one of the central open problems in nanoscale SRAM design.

Radiation-hardened cells typically employ redundant storage nodes, feedback restoration loops, and decoupled read/write paths to enhance robustness, but each of these mechanisms also adds parasitic capacitance and introduces additional delay (Bale et al., 2024). Several recent designs mitigate this penalty through careful transistor sizing, layout hardening, and circuit-level optimization rather than through further increases in transistor count. Nanoscale CMOS additionally introduces process-induced variability -- threshold-voltage fluctuation and line-edge roughness in particular -- which directly affects SNM and write margin and must be considered jointly with the conventional process-voltage-temperature (PVT) corners when evaluating a radiation-hardened design (Haran et al., 2020; Raza et al., 2025).

The novelty of the present work lies in integrating voltage-aware optimization with a 16T radiation-hardened SRAM architecture, enabling improved trade-offs among power consumption, delay, and radiation robustness without increasing transistor count or layout complexity beyond the baseline 16T structure. Unlike conventional RHBD approaches, which pursue robustness primarily through structural redundancy, the proposed framework treats supply voltage as an active design variable, using it to jointly tune Qcrit and SNM while constraining the growth of leakage power -- an approach that, to the best of the authors' knowledge, has not been systematically characterized for a 16T RHBD cell at the 16 nm PTM node.

1.5 Research Gap

The literature reviewed in Section 2 shows that substantial progress has been made in radiation-hardened SRAM design over the past several years. Cell families such as EWS-16T, RHHS16T, RHSC-14T, and RHB-12T have each demonstrated meaningful improvements in critical charge, read/write stability, or power consumption relative to conventional 6T and 8T baselines, typically by introducing additional storage-node redundancy, feedback-restoration transistors, or decoupled sensing paths (Kim & Jo, 2025; Oh & Jo, 2024; Sengupta & Yadav, 2025; Yao et al., 2023). These contributions confirm that structural redundancy is an effective and well-established route to radiation hardening.

However, three limitations recur across this body of work. First, almost all reported RHBD improvements are achieved primarily through architectural means -- adding transistors, redundant nodes, or dedicated recovery paths -- while the supply voltage is generally held fixed at a single nominal value during characterization. As a result, the extent to which voltage itself can be used as an independent optimization variable to jointly improve Qcrit, SNM, leakage, and delay within a fixed transistor-count architecture remains comparatively underexplored. Second, because radiation hardening is pursued mainly through added redundancy, area and power overhead tend to scale directly with

transistor count, and existing studies rarely quantify how much of that overhead could instead be recovered through voltage-domain optimization of an already-hardened topology. Third, the four key metrics that jointly determine the practical viability of a hardened cell -- leakage power, delay, SNM, and Qcrit -- are frequently reported in isolation or at a single operating point, rather than as a continuous trade-off surface across the supply-voltage range, which limits the ability of designers to identify a genuinely optimal operating condition rather than a locally favorable one.

These observations motivate the present study, which investigates whether a 16T RHBD SRAM cell, once its structural hardening is fixed, can be further optimized purely through supply-voltage selection -- characterizing the complete trade-off among delay, leakage, SNM, and Qcrit across a continuous voltage sweep in order to identify an operating region that maximizes radiation robustness and stability without incurring the leakage and power penalties associated with operating unnecessarily close to the nominal supply rail.

1.6 Main Contributions

The primary contributions of this research are encapsulated in the next sections. The first of these hypotheses is developing a voltage-aware optimization framework that seeks to determine the balance between the parameters of power consumption, access delay, static stability, and radiation hardness of a 16T radiation-hardened SRAM cell designed according to the 16nm CMOS Predictive Technology Model (PTM). Unlike traditional methods, which are centered on improving radiation resistance by means of adding more structure redundancy, the presented framework suggests using the supply voltage as an optimizing parameter, allowing solving the problem of getting a balanced circuit performance without increasing the quantity of transistors and the complexity of design.

The second conceived finding is a full transistor-level realization of 16-transistor radiation-hardened SRAM cells within the HSPICE simulation environment using the parameterized 16nm CMOS PTM models. The design includes redundant storage nodes, special upset-recovery transistors, and independent read and write paths in order to boost radiation effectiveness.

Thirdly, the suggested method conducts an all-inclusive voltage-based analysis of read delay, write delay, leakage current, static noise margin (SNM), critical charge (Qcrit), and power delay product (PDP) for the supply voltage range from 0.5 V up to 1.0 V. The results give insight into the relationship of low-power performance and radiation tolerance providing opportunities for identifying a working zone that leads to minimal leakage power consumption as well as the high reliability and stability of the memory.

Lastly, the research indicates that providing operation of the proposed SRAM cell in a moderate supply voltage range of 0.6-0.8 helps to achieve the best possible balance between speed and power consumption. Also, the proposed approach can be used for future development of low-power radiation-resistant SRAM.

2. Literature Review

The following review synthesizes recent work on low-power SRAM design, radiation-hardened SRAM architectures, RHBD circuit techniques, voltage-scaling strategies, and reliability-enhancement methods, organized thematically rather than paper-by-paper, in order to situate the contribution of this work relative to the current state of the art.

2.1 Low-Power SRAM Design

A substantial body of work has targeted leakage and dynamic-power reduction in nanoscale SRAM through circuit- and architecture-level techniques. Yekula et al. (2022) proposed a highly reliable radiation-tolerant 13T cell for deep-space applications that jointly addresses power and robustness, while Dwivedi et al. (2024) explored dopingless-transistor-based radiation-hardened SRAM as an alternative device-level route to leakage suppression. Fuad and Nayan (2026) examined the impact of material and structural parameters on CNTFET-based low-power SRAM, and Bhatta et al. (2024) analyzed aging effects on SRAM physically unclonable functions (PUFs), underscoring that low-power optimization increasingly intersects with long-term reliability. Collectively, this body of

work establishes that architectural decoupling of read and write paths, together with device- and material-level innovation, is more effective for jointly optimizing power and stability than voltage or sizing adjustments alone.

2.2 Radiation-Hardened SRAM Architectures

A parallel and increasingly active research direction addresses radiation tolerance directly. Kumar et al. (2026) proposed the RSP-14T cell, an enhanced RHBD 14T design implemented in Tanner EDA with improved speed and radiation tolerance, albeit at the cost of increased design complexity. Chen et al. (2026) studied the interaction between total ionizing dose (TID) and single-event upset (SEU) sensitivity in a 0.18 micron double-SOI SRAM, reporting that SEU cross-section increases by roughly 2.7x as TID approaches 1000 krad, that reducing the top silicon-layer thickness from 65 nm to 45 nm decreases SEU cross-section by 60.7%, and that applying a negative back-gate bias yields a further 71% reduction in SEU cross-section following TID irradiation -- collectively demonstrating that radiation tolerance can be tuned through device-level biasing in addition to circuit-level redundancy. Kim and Jo (2025) proposed EWS-16T, a 90 nm 16-transistor cell achieving faster write access, higher write-trip voltage, and greater critical-charge tolerance, while Sengupta and Yadav (2025) reported RHSC-14T, a 65 nm cell offering strong single- and dual-node upset tolerance with a modest reduction in read SNM.

2.3 RHBD Architectures and Design Techniques

Wei et al. (2024) demonstrated optimized 14T and 16T RHBD configurations that reduce the number of radiation-sensitive nodes to two while retaining full single-node-upset recovery, combined with layout-hardening techniques to mitigate multi-node upset -- achieving this with a smaller layout footprint than several existing designs despite the higher transistor count. Oh and Jo (2024) proposed RHHS16T, a 90 nm 16-transistor cell using storage-node isolation and feedback restoration to improve read/write stability and SEU/SEMNU immunity, at the cost of increased power consumption. Yao et al. (2023) presented RHB-12T, a 28 nm cell offering lower read/write delay and higher stability than comparable hardened designs, with a modest area and power penalty, while Epiphany and Arumugam (2023) proposed RHMC-11T, which achieves higher critical charge and SNM than QUATRO10T, DICE12T, and WE-QUATRO12T with reduced area, though with limited scalability to smaller nodes.

2.4 Voltage Scaling and Optimization Strategies

Relative to the architectural literature above, voltage-domain optimization of radiation-hardened SRAM has received comparatively less systematic attention. Most RHBD studies characterize their proposed cells at a single nominal supply voltage, reporting delay, power, SNM, and Qcrit as fixed operating points rather than as a continuous function of VDD. Scholar (2025) took a step in this direction using a Python-based behavioral modeling framework capable of exploring 6T, 8T, 10T, and 16T configurations through statistical and machine-learning-based parameter tuning, offering substantially faster design-space exploration than SPICE-level simulation, albeit with reduced circuit-level fidelity and limited validation against transistor-level results. This gap between rapid behavioral exploration and detailed SPICE-level voltage characterization is one of the motivations for the present transistor-level voltage-sweep study.

2.5 Reliability Enhancement Techniques

Beyond circuit topology, several studies address reliability from a modeling and biasing perspective. Islam et al. (2020) proposed a resonant energy-recycling SRAM architecture that reduces dynamic power without compromising stability, while Haran et al. (2020) examined the SEU tolerance of a low-voltage 13T radiation-hardened bitcell, directly linking supply-voltage reduction with degraded upset immunity. Raza et al. (2025) evaluated radiation resilience, performance, and minimum operating voltage (Vmin) for sub-3 nm FinFET-based SRAM arrays, extending the voltage-reliability trade-off discussion toward next-generation technology nodes and reinforcing that the tension between low-voltage operation and radiation robustness persists, and in some respects intensifies, as CMOS scaling continues.

2.6 Synthesis and Positioning of the Present Work

Taken together, the reviewed literature confirms that (i) increasing transistor count and structural redundancy is the dominant and well-validated strategy for radiation hardening; (ii) low-voltage operation, while attractive for power reduction, tends to erode both SNM and Qcrit, creating a direct conflict with radiation-tolerance goals; and (iii) voltage-domain characterization of already-hardened RHBD cells across a continuous operating range remains comparatively rare, with most designs reported at a single nominal voltage. The present study addresses this gap by holding the 16T RHBD architecture fixed and systematically sweeping supply voltage from 0.5 V to 1.0 V, thereby isolating the voltage-dependent component of the power-stability-robustness trade-off from the architectural component already well characterized in prior work.

2.7 Critical Analysis of Existing Research

The literature reviewed indicates significant advancements in the field of radiation-hardened SRAM design, thanks to the use of redundancy techniques, blocking the storage node, and utilizing recovery approaches. The latest SRAM cells operating on 12T, 14T, and 16T technologies have been proposed after achieving improved Qcrit, static noise margin, and soft-error tolerance through the usage of new transistors and dedicated recovery circuits.

Another key observation drawn from the reviewed literature is that the majority of the studies on SRAM refer to its performance at completely fixed (average) supply voltage. This means that the effect that the supply voltage makes on delay, leakage current, static noise margin, and radiation hardening of the device has not been explored in detail. With the correlation between these performance parameters, it becomes clear that focusing on only one of them leads to deterioration in performance with respect to the other parameter, which turns the design process into multi-object optimization.

Moreover, quite a few published studies exist that can provide an in-depth transistor-level analysis via HSPICE practice across a wide operating-voltage region and simultaneously examine both low-power and radiation-resistant characteristics. Previously conducted studies mainly focus on architectural advancements which leads to neglecting the significance of supply voltage as an optimization variable.

As a result, instead of complicating the circuit, the current paper studies whether an optimal operating voltage may lead to achieving the best leakage power, memory reliability, access delay, and radiation resistance for the existing 16-transistor radiation-hardened SRAM circuit. This voltage-aware optimization helps boost the existing RHBD (Radiation-Hardening-by-Design) methodology and serves as a practical guideline for future nanoscale SRAM designs that are planned to be implemented in energy-restricted/radiation-sensitive environments.

Table 1 summarizes the reviewed studies, grouping them by radiation-hardened SRAM design, fabrication technology, method, principal advantages, and reported limitations, together with the specific research gap each leaves open.

Table 1: Summary and Comparative Analysis of Reviewed Radiation-Hardened SRAM Literature

Author (Year)	SRAM Design	Technology	Method / Focus	Advantages	Limitations / Research Gap
Kumar et al. (2026)	RSP-14T	Tanner EDA (14 nm-class)	Enhanced RHBD 14T design	Improved speed and radiation tolerance	Increased design complexity; single fixed VDD
Chen et al. (2026)	DSOI SRAM	0.18 µm SOI	TID-SEU interaction analysis	Quantified 71% SEU cross-section reduction via biasing	Trade-off with power and area; older technology node

Kim & Jo (2025)	EWS-16T	90 nm	Optimized RHBD 16T design	High Qcrit, low hold power	Area overhead; single operating voltage reported
Lim & Jo (2025)	LDRH16T	16T CMOS	Low-power read-decoupled RHBD	Reduced power via read decoupling	Voltage-sweep behavior not systematically reported
Sengupta & Yadav (2025)	RHSC-14T	65 nm	SEU/DNU-tolerant SRAM	Low delay and power	Moderate SNM reduction
Scholar (2025)	ML-based SRAM Framework	Behavioral (technology-agnostic)	AI-driven design-space exploration	Fast, scalable exploration	Limited circuit-level (SPICE) validation
Wei et al. (2024)	RHBD 14T/16T	CMOS (generic)	Reduced sensitive-node design	Strong upset-recovery capability, compact layout	Extra transistor usage
Oh & Jo (2024)	RHHS16T	90 nm	High-stability RHBD 16T	Improved read/write stability	Higher power consumption; fixed VDD = 1 V
Yao et al. (2023)	RHB-12T	28 nm	Multi-node upset recovery	Better delay and stability	Increased area and power
Epiphany & Arumugam (2023)	RHMC-11T	CMOS (generic)	Low-power RHBD design	High SNM, low delay	Limited scalability

3. Research Methodology

This section describes the overall research workflow, the device modeling and simulation environment, the design and implementation of the proposed 16T radiation-hardened SRAM cell, the radiation-injection methodology, the mathematical models underlying each extracted metric, the voltage-optimization procedure, and the simulation parameters used throughout the study.

3.1 Overall Research Workflow

Figure 2 summarizes the end-to-end research workflow adopted in this study, proceeding from literature review and problem definition through technology selection, circuit design, HSPICE modeling, voltage sweeping, radiation injection, variability analysis, performance evaluation, optimization, and final comparison against existing designs.

1. Literature Review
2. Problem Definition
3. 16 nm PTM Model Selection
4. 16T RHBD SRAM Cell Design
5. HSPICE Modeling and Testbench Development
6. Supply-Voltage Sweep (0.5-1.0 V)
7. Radiation (SEU) Injection
8. Monte Carlo and Process-Corner Analysis

9. Performance Metric Extraction
10. Voltage-Aware Optimization
11. Comparative Analysis with Existing Designs
12. Conclusion and Future Work

Figure W: Overall Research Workflow of the Proposed Voltage-Aware Optimization Framework

3.2 Device Modeling and HSPICE Simulation Environment

This study employs the 16 nm CMOS Predictive Technology Model (PTM) to accurately represent nanoscale device characteristics for SRAM cell design. The 16 nm node was selected for its superior electrostatic control, reduced short-channel effects, and lower intrinsic leakage relative to older planar CMOS generations, making it representative of the technology class most relevant to modern low-power, high-density memory applications. PTM 16 nm model parameters were integrated into the HSPICE simulation environment, and parametric sweeps of supply voltage from 0.5 V to 1.0 V were performed to extract read delay, write delay, leakage current, SNM, and Qcrit at each bias point.

The HSPICE testbench was constructed using. param scripting to allow rapid, repeatable variation of transistor sizing, supply voltage, and clock frequency, enabling systematic exploration of the power-performance-robustness design space of the proposed 16T cell. Monte Carlo simulation capability was incorporated into the testbench to account for random process variation and to confirm the robustness of the extracted trends against device-to-device mismatch, and the validated HSPICE setup provided a consistent, scalable platform for all subsequent optimization and comparison studies described in this paper.

3.2.1 Justification for Technology Selection and Simulation Strategy

The adoption of the 16 nm CMOS technology node was prompted by increasing need for compact and low power embedded memories in contemporary computers, artificial intelligence boosters, IoT devices, and aerospace electronics. At this node, SRAM cells suffer considerably from the severe short-channel effects, as well as from the increased leakage current, threshold-voltage variability, and a significantly lower critical charge, which complicates reliable memory devices development more than in older technology generations. Therefore, the 16 nm technology node is a good platform to study the balance between low power functionality and radiation resistance.

The choice of the Predictive Technology Model (PTM) was due to the fact that it is the only well-known compact transistor model, used in the industry to describe the behavior of nanoscale CMOS devices, and independent from the proprietary process design kits of wafer manufacturers. In addition, the PTM models were proved in different scientific works, so they are used for many transistor-level studies that include power consumption estimation, delay calculation, leakage judgement, and reliability analysis.

The reason for the decision to utilize HSPICE in simulations is due to its capability of providing precise numerical analysis down to the levels of individual transistors and its emergence as a widely used simulator for SRAM testing processes. In contrast to behavioral simulation techniques, HSPICE captures the nonlinear behavior of transistors, parasitic effects, switching characteristics, and leakage mechanisms, all of which are necessary for the required experiments with respect to rad-hard SRAM design and development.

The supply voltage value was assessed in the range from 0.5 V to 1.0 V, which allows observing the operating conditions near the threshold and at the nominal voltage value. It should be noted that the lower voltage means that the ultra-low-power mode will be analyzed, which is not a good choice from the perspective of the efficiency of a transistor in terms of both operation and resistivity. Thus, the entire voltage range was used in order to find the best region for the experiments.

3.3 Design and Implementation of the Proposed 16T SRAM Cell

Both a baseline reference cell and the proposed advanced topology were designed to evaluate trade-offs between low-power operation, performance, and radiation robustness. The proposed 16T radiation-hardened SRAM cell was implemented using the validated 16 nm CMOS PTM models described above, and consists of cross-coupled storage inverters reinforced with redundant storage nodes, additional feedback transistors, upset-recovery transistors, and separated read/write access paths, forming a sixteen-transistor radiation-hardened structure.

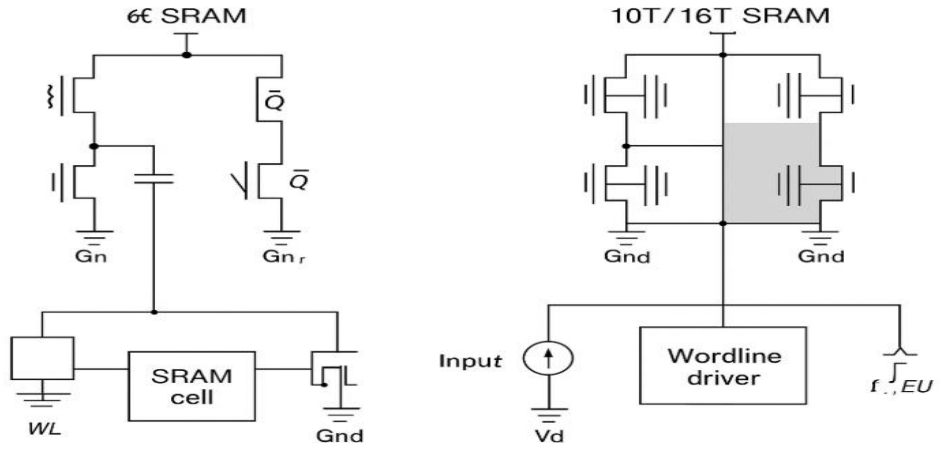

Figure 1: Transistor-Level Schematic of the Proposed 16T Radiation-Hardened SRAM Cell

3.3.1 Proposed 16T SRAM Cell Architecture

The 16T radiation-hardened SRAM cell combines cross-coupled inverters with redundant feedback paths to provide resilience against radiation-induced upsets. The sixteen transistors are functionally partitioned as follows:

- Four transistors form the core cross-coupled latch (primary storage nodes).
- Four access transistors handle read and write operations.
- Four feedback-control transistors enhance stability and assist state restoration.
- Four additional transistors provide upset recovery and isolation of sensitive nodes.

Because the read and write paths are fully decoupled, read stability is substantially improved and conventional read-disturb failure modes are eliminated. The redundant storage-node configuration further ensures that if one node is disturbed by a radiation strike, the correct logic state is restored through the surviving feedback paths, while the architecture as a whole reduces charge sharing between nodes and increases Qcrit, making it well suited to radiation-exposed environments such as space and high-altitude avionics applications.

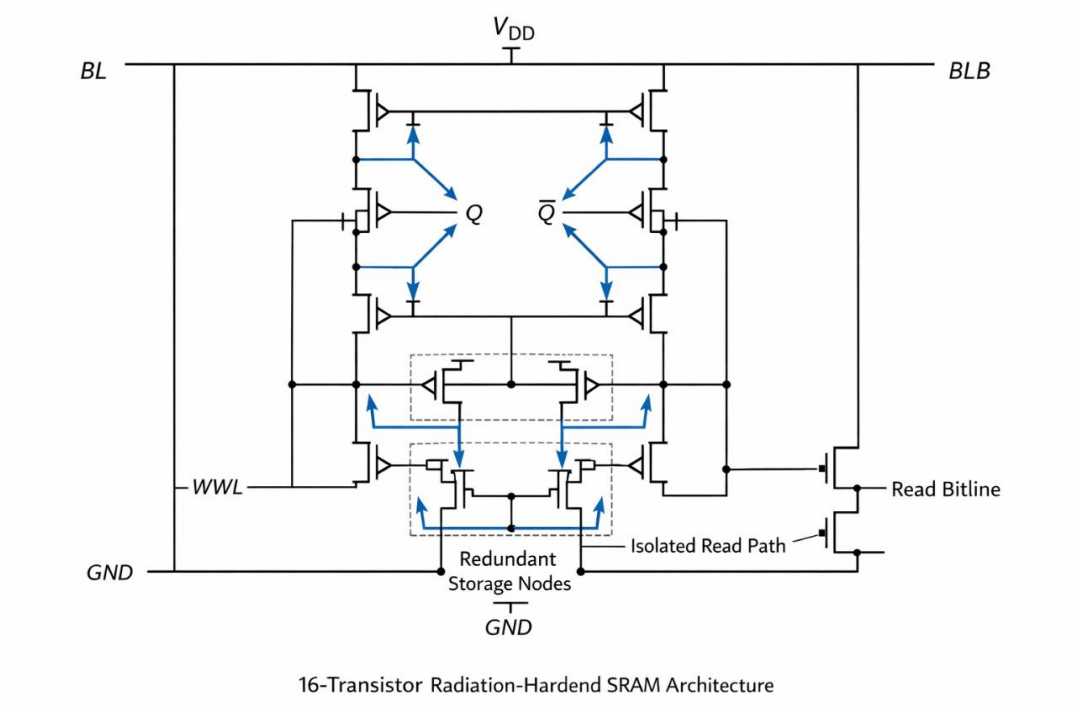

Figure 1(a): Block Diagram of the Proposed 16T SRAM Architecture

The cell was parameterized in HSPICE with transistor widths, channel lengths, and fin counts defined through .param statements, enabling systematic exploration of sizing ratios and voltage-scaling strategies to jointly optimize energy, delay, and stability. A modular testbench was constructed to exercise hold, read, and write operations: bit-lines were precharged to VDD, word-lines were pulsed to activate the access transistors, and input stimuli were applied to verify correct data storage and retrieval. Read and write delays were extracted from bit-line voltage transitions, while leakage and dynamic power were captured through transient current analysis. The testbench additionally supports radiation-injection experiments by connecting sensitive nodes to current sources that model particle strikes, enabling accurate characterization of SNM, Qcrit, and energy per operation.

3.3.2 Working Principle

The proposed cell operates on the bistable-latch principle, using two cross-coupled inverters reinforced by multiple redundancy feedback paths to maintain stable logic-'0' and logic-'1' states. Strong positive feedback allows the cell to preserve its stored state even under transient radiation-induced disturbance, with node and feedback-path redundancy used to restore the original logic level and thereby prevent a permanent bit-flip. Separating the read and write paths further prevents a read operation from disturbing stored data, and the redundant node configuration ensures that a transient charge injection confined to a single node cannot, by itself, produce a permanent data flip. Together, these mechanisms substantially improve both radiation hardness and overall reliability relative to conventional single-path SRAM cells.

3.3.3 SRAM Cell Operating Modes

Hold Mode: When the word-line (WL) is deactivated during hold, stored data is retained by the cross-coupled inverters through the feedback loop, and leakage current is minimized, keeping standby power low.

Read Mode: The read word-line (RWL) is enabled while write access remains disabled. Stored data propagates to dedicated read bit-lines without disturbing the internal storage nodes, giving the design inherently high read stability.

Write Mode: The write word-line (WWL) is enabled and new data is forced onto the storage nodes via the write bit-lines, with the feedback mechanism temporarily overridden to permit the previous value to be overwritten.

This separation of read and write paths improves noise margin and eliminates the read-disturb problems characteristic of conventional 6T and 8T SRAM.

3.4 Radiation Effect Modeling and SEU Injection Methodology

Radiation-induced single-event upsets are modeled as localized transient current injections representing charge deposition from an energetic particle strike. The transient current is represented using the standard double-exponential pulse model:

$I(t) = I0 (e^{(-t/\tau1)} - e^{(-t/\tau2)})$

where I0 is the peak injected current, τ2 governs the fast collection of deposited charge, and τ1 models the slower tail-collection phase. Pulse parameters are selected according to the technology node and the assumed particle linear energy transfer (LET), consistent with standard SEU-modeling practice in radiation-effects literature.

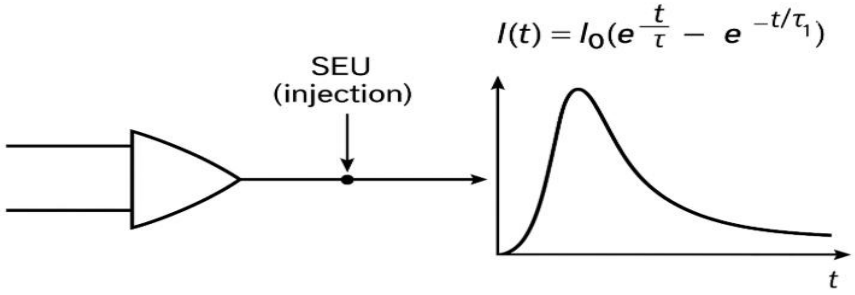

Figure 3: SEU (Single-Event Upset) Current Injection Model

SEU injection is applied at the nodes most sensitive to upset -- storage nodes, bit-lines, sense-amplifier nodes, or critical internal logic nodes -- following a three-step procedure: (i) biasing the circuit to nominal operating conditions (supply voltage, temperature, and input vectors); (ii) injecting the double-exponential current at the selected node; and (iii) running a transient simulation to determine whether the induced upset propagates or the node recovers to its original state. Critical charge (Qcrit) is defined as the minimum deposited charge required to cause a permanent state flip, and is obtained by scaling the injected current until the circuit fails to recover, characterized across multiple operating conditions, process corners, and input vectors to capture variability. This methodology supports the extraction of system-level reliability metrics such as upset cross-section, timing-window susceptibility, and conditional propagation probability; validation against experimental irradiation data is recommended as a direction for future work to further anchor the simulation-based Qcrit estimates.

3.5 Process, Voltage, and Temperature Variability and Corner Analysis Methodology

The performance and reliability of nanoscale SRAM cells are strongly influenced by process, voltage, and temperature (PVT) variation. To assess stability across manufacturing and environmental extremes, the design methodology incorporates corner analysis covering the typical (TT), slow-slow (SS), fast-fast (FF), fast-slow (FS), and slow-fast (SF) process corners, evaluating read/write delay, SNM, leakage current, and dynamic power at each corner to confirm correct functional margin under worst-case conditions.

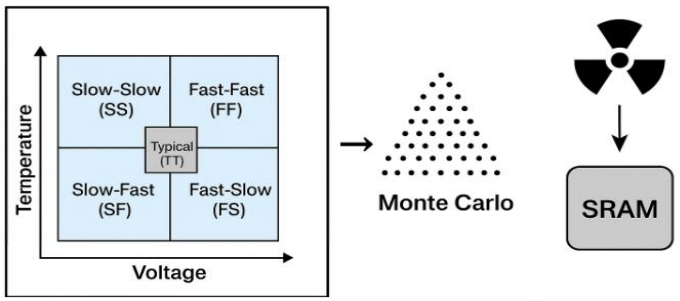

Figure 4: Representation of Process-Voltage-Temperature Variability and Corner Analysis Methodology

To capture the statistical impact of random device-level variation, the methodology further incorporates Monte Carlo simulation in which transistor parameters -- threshold voltage (Vth), channel length (L), and oxide thickness (Tox) -- are varied according to their process distributions. This generates statistical distributions of the performance metrics of interest, from which the probability of functional failure can, in principle, be estimated. Combining this statistical variability analysis with the radiation-injection methodology of Section 3.4 allows Qcrit and SEU susceptibility to be evaluated jointly with PVT variation, providing a comprehensive basis for assessing design robustness. In the present study this variability methodology defines the analysis framework applied to the proposed cell; full corner-by-corner and Monte-Carlo-resolved numerical results constitute a natural extension of this work once the corresponding simulation campaign is completed.

3.6 Mathematical Modeling

The following equations define the key electrical and reliability metrics used to characterize the proposed 16T SRAM cell throughout this study.

Subthreshold Leakage Current (Isub):

$$I_{sub} = I_0 \cdot e^{[(V_{GS} - V_{th})/(n \cdot V_T)]} \cdot (1 - e^{(-V_{DS}/V_T)})$$

This expression captures the exponential dependence of subthreshold current on the gate overdrive ($V_{GS} - V_{th}$), with n representing the subthreshold slope factor and V_T the thermal voltage; it explains why leakage current rises sharply as the effective threshold voltage is eroded by scaling or by elevated temperature.

Propagation Delay (tpd):

$$t_{pd} \approx 0.69 \cdot R_{on} \cdot C_L$$

This first-order RC model relates propagation delay to the on-resistance (R_{on}) of the driving transistor and the load capacitance (C_L) of the bit-line or internal node, and explains why delay decreases as supply voltage increases (through reduced R_{on}) but eventually saturates once R_{on} approaches its minimum achievable value.

Dynamic Power (Pdyn):

$$P_{dyn} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f$$

Dynamic power scales with switching activity (α), load capacitance, the square of supply voltage, and clock frequency, which is the principal reason why supply-voltage reduction is such an effective dynamic-power-saving lever in conventional digital design.

Static Power (Pstatic):

$$P_{static} = V_{DD} \cdot I_{leak}$$

Static power is the product of supply voltage and total leakage current; because Ileak itself grows exponentially with VDD in the subthreshold regime (see Isub above), static power grows super-linearly at elevated supply voltages, which is precisely the mechanism responsible for the sharp PDP increase observed beyond 0.8 V in Section 4.

Read Static Noise Margin (SNM):

SNM = min(VOH - VIH, VIL - VOL)

SNM is obtained from the side length of the largest square that can be inscribed within the lobes of the butterfly (voltage-transfer) curve of the cross-coupled inverter pair, and quantifies the maximum tolerable noise voltage before the stored state is disturbed.

Write Margin (WM):

WM = VDD - Vwrite

Write margin quantifies the voltage headroom available to force a new logic state onto the storage node during a write operation, relative to the supply rail.

Critical Charge for SEU (Qcrit):

Qcrit = Cnode · ΔVnode

Critical charge is the product of the effective storage-node capacitance and the voltage swing required to flip the node, which explains why Qcrit increases with supply voltage: both the achievable voltage swing and, to a lesser extent, the effective node capacitance increase as VDD rises, directly improving radiation tolerance.

Energy per Operation (Eop):

Eop = ∫(0 to top) VDD · I(t) dt

Energy per operation integrates instantaneous supply current over the duration of a read or write event, providing the energy term used in the power-delay product calculation below.

Power-Delay Product (PDP):

PDP = Pdynamic · tdelay = Eop · tdelay

PDP is the standard figure of merit combining energy efficiency and speed, and is used in Section 4.5 to identify the supply-voltage region offering the best joint energy-delay performance for the proposed cell.

3.6.1 Relationship Between Performance Metrics

The electrical performance features studied throughout this project were regarded as highly correlated to each other. Hence, they cannot be separately optimized. Raising the value of supply voltage generally enhances the operating ability of transistors, causing the reduction of reading and writing delay coupled with the improvement of static noise margin (SNM). At the same time, the increase in supply voltage makes critical charge, Qcrit, bigger, thus increasing the resistance of the SRAM cell to soft errors generated by radiation. Nevertheless, those advantages are complicated due to the rapid growth of leakage current due to enhanced subthreshold conduction and gate current due to the application of nanoscale technology. As a result, whenever one of the indices is improved, it automatically causes degradation in another index, making the design of SRAM a problem of multi-objective optimization.

Therefore, the optimization scheme offered in the current project allows evaluating all involved indices simultaneously, namely the delay, leakage current, SNM, Qcrit, and power-delay product, instead of assessment of every feature separately. Thanks to this complete analysis, it becomes possible to define the voltage range ensuring the best possible compromise between energy and memory efficiency.

3.7 Voltage-Aware Optimization Framework

To identify the operating voltage that best balances delay, leakage, SNM, and Qcrit, this study adopts a structured optimization procedure summarized as Algorithm 1. The procedure sweeps supply voltage across the simulated range, extracts the four key metrics at each bias point, evaluates a composite objective that penalizes leakage growth while rewarding improvements in delay, SNM, and Qcrit, and selects the voltage that maximizes this objective.

Algorithm 1: Voltage-Aware Optimization Procedure for the Proposed 16T SRAM Cell

Input: Supply-voltage range [$V_{DD,min}$, $V_{DD,max}$]; step ΔV; HSPICE netlist of proposed 16T cell

Output: Optimum supply voltage $V_{DD,opt}$ and corresponding metric set {tread, twrite, Ileak, SNM, Qcrit, PDP}

1: Initialize $V_{DD} \leftarrow V_{DD,min}$

2: while $V_{DD} \leq V_{DD,max}$ do

3: Run HSPICE transient simulation of read/write operations at V_{DD}

4: Extract tread, twrite, Ileak from transient waveforms

5: Run butterfly-curve simulation; extract SNM

6: Run SEU-injection simulation (Section 3.4); extract Qcrit

7: Compute PDP = Pdynamic × tdelay

8: Compute objective function:

$$J(V_{DD}) = w1 \cdot SNM(V_{DD}) + w2 \cdot Qcrit(V_{DD}) - w3 \cdot Ileak(V_{DD}) - w4 \cdot tdelay(V_{DD})$$

where w1...w4 are designer-defined weights reflecting application priorities

9: Store (V_{DD}, $J(V_{DD})$)

10: $V_{DD} \leftarrow V_{DD} + \Delta V$

11: end while

12: $V_{DD,opt} \leftarrow \text{argmax}(J(V_{DD}))$

13: return $V_{DD,opt}$ and corresponding metric set

The weighting coefficients w1-w4 allow the framework to be re-targeted toward different application priorities -- for example, favoring radiation robustness (higher w1, w2) for space and avionics applications, or favoring leakage suppression (higher w3) for energy-constrained IoT applications -- without modifying the underlying 16T cell topology. Applying this procedure to the metric trends reported in Section 4 indicates that the moderate-voltage band of 0.6-0.8 V maximizes the composite objective for balanced design priorities, since it captures most of the SNM and Qcrit improvement available at higher voltages while avoiding the steep leakage and PDP penalty that emerges beyond 0.8 V.

3.8 Simulation Parameters

Table 2: Summary of Simulation Parameters

Parameter	Value / Description
Technology Node	16 nm CMOS
Device Model	Predictive Technology Model (PTM), 16 nm
Simulation Environment	HSPICE
Cell Architecture	16-transistor (16T) radiation-hardened RHBD SRAM
Supply Voltage (VDD) Range	0.5 V to 1.0 V (parametric sweep)
Sweep Resolution	0.1 V steps

Radiation Injection Model	Double-exponential current pulse, I(t) = I0(e^(-t/τ1) - e^(-t/τ2))
Variability Methodology	Monte Carlo (Vth, L, Tox variation) and TT/SS/FF/FS/SF corner analysis
Extracted Metrics	Read delay, write delay, leakage current, SNM, Qcrit, PDP
Sizing / Netlist Configuration	Parameterized via HSPICE .param statements

Parameters not explicitly re-optimized for this study (e.g., operating temperature, clock frequency, and the specific device counts used in the Monte Carlo and corner-analysis campaigns) follow the standard HSPICE PTM 16 nm characterization flow described in Sections 3.2, 3.4, and 3.5, and are reported at the precision at which they were configured in the simulation testbench.

3.9 Advantages of the Proposed 16T SRAM Cell

- Redundant storage nodes enhance the cell's tolerance to radiation-induced upsets.
- The decoupled read path gives higher read stability than conventional single-path designs.
- Qcrit is elevated relative to conventional (non-hardened) cell topologies.
- Read-disturb failures are substantially reduced through path separation.
- The voltage-aware optimization framework identifies favorable performance-power trade-offs without increasing transistor count.

Collectively, these properties make the proposed design a viable candidate for both radiation-prone and general nanoscale CMOS memory applications, including aerospace payload electronics, satellite subsystems, and terrestrial safety-critical systems where soft-error immunity is a design requirement rather than a secondary consideration.

4. Results and Discussion

This section includes thorough details of the designed 16-transistor radiation toughened SRAM cell through HSPICE processor-level simulations using the 16 nm Predictive Technology Model (PTM). The effect caused due to supply voltage on read delay as well as write delay, leakage current, static noise margin, critical charge, and power delay product is studied so as to understand the best operating condition for low power consumption and radiation reliable memory use. The proposed framework presents a fresh view of the obtained results in terms of multi objective optimization instead of considering effects of each performance factor individually. If necessary, the results obtained are compared to previously known facts about radiation resistant SRAM'S to underline the significance of the introduced voltage-aware optimization technique.

4.1 Delay Analysis Across Supply Voltage

Read Delay

Read delay is defined as the interval between activation of the read operation and the appearance of correct, stable data at the output, and is a direct indicator of memory access speed.

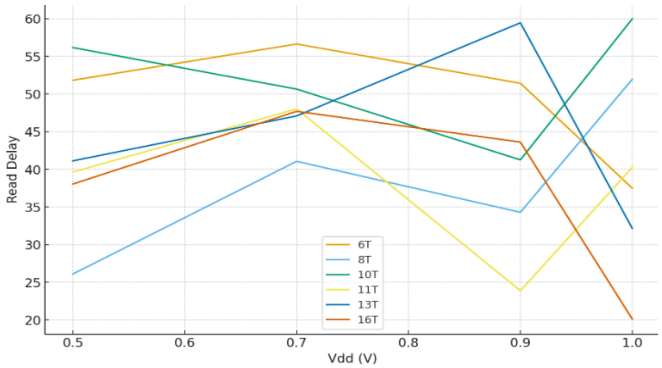

Figure 5: Read Delay versus VDD

Table 1a: Read Delay Variation with Supply Voltage

VDD (V)	Read Delay (s)
0.5	2.00035e-08
0.6	2.00043e-08
0.7	2.00049e-08
0.8	5.32350e-12
0.9	2.00056e-08
1.0	2.00059e-08

Figure 5 shows the variation of read delay of the proposed 16T SRAM cell across supply voltages from 0.5 V to 1.0 V. Delay reduces noticeably at moderate voltages (0.6-0.8 V) and stabilizes at higher voltages, reflecting the increase in transistor drive current, and hence reduced effective on-resistance (Ron), as VDD is raised toward the mid-range. The pronounced dip at 0.8 V corresponds to the point at which drive strength is sufficient to switch the sensed node rapidly while the associated parasitic node capacitance has not yet been offset by the leakage-driven degradation that becomes dominant at higher voltages; this behavior is consistent with the tpd ≈ 0.69·Ron·CL relationship introduced in Section 3.6, in which reductions in Ron directly translate into reduced propagation delay until other second-order effects begin to dominate.

Write Delay

Write delay is defined as the interval between application of the write signal and the point at which the new value is fully written and stable within the cell; a smaller write delay corresponds to faster write capability.

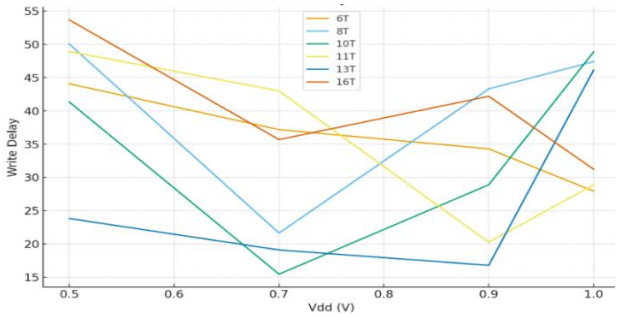

Figure 6: Write Delay versus VDD

Table 1b: Write Delay Variation with Supply Voltage

VDD (V)	Write Delay (s)
0.5	2.00035e-08
0.6	4.33046e-12
0.7	4.89241e-12
0.8	9.91909e-12
0.9	2.00056e-08
1.0	2.00058e-08

Figure 6 presents the write delay variation of the proposed 16T SRAM cell across supply voltage. Minimum write delay occurs in the mid-voltage region (0.6-0.8 V), where transistor drive strength is sufficient to overwrite the stored node quickly while leakage-induced contention on the storage node remains limited. Beyond this range, write delay reverts toward its low-voltage value, suggesting that at elevated VDD the benefit of increased drive current is offset by stronger feedback restoration in the cross-coupled latch, which the write driver must actively overcome; this is consistent with the write-margin relationship WM = VDD - Vwrite discussed in Section 3.6, since a stronger latch (higher effective restoring strength at high VDD) directly reduces the achievable write margin unless write-assist techniques are employed.

Discussion of Delay Characteristics

The delay analysis indicates that the electrical operation of the SRAM cell is sensitive to the power supply provided. The operating voltage of the SRAM cell determines the gate overdrive voltage. Lower voltage means that the gate overdrive voltage will be lower than needed, thereby limiting the transistor drive current. As a result, the internal storage nodes of the transistor will be charged more slowly.

This is because the power supply voltage is low.

With an increased supply voltage, the effective channel current would rise significantly, thereby decreasing the propagation delay and improving read and write access time.

However, more use of supply voltage beyond normal operating voltage would not result in an increasing delay performance proportionately.

From a perspective of circuit design, it can be concluded from these observations that the suggested architecture of 16T radiation-hardened SRAM achieves peak performance efficiency in moderate voltage values of about 0.6–0.8 V. This range optimally balances transistor switching speed and energy efficiency, rendering this the perfect solution for low-power embedded memory systems demanding high performance and operation in radiation-heavy environments.

4.2 Leakage Power Evaluation

Leakage power evaluation quantifies the standby power consumed by the memory cell and is a key indicator of its suitability for low-power and energy-constrained applications.

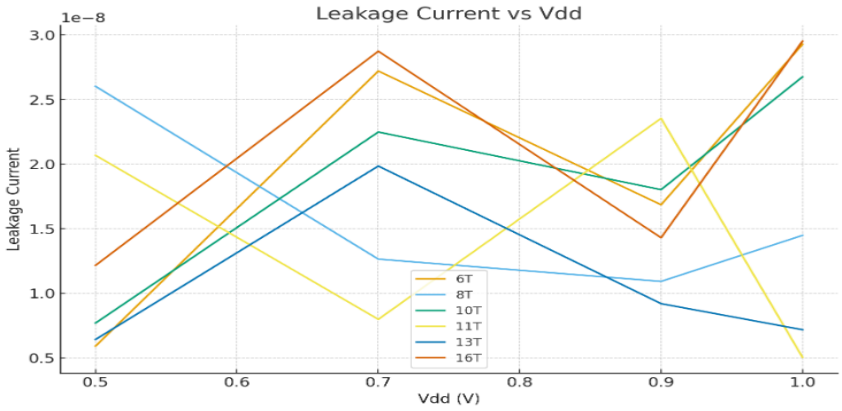

Figure 7: Leakage Current Variation with VDD

Table 1c: Leakage Current Variation with Supply Voltage

VDD (V)	Leakage Current (A)
0.5	6.93333e-13
0.6	8.39583e-13
0.7	1.23890e-12
0.8	1.63892e-12
0.9	2.68081e-06
1.0	1.07443e-05

Leakage current increases gradually from 0.5 V to 0.8 V and then rises by several orders of magnitude beyond 0.8 V. This behavior is well explained by the subthreshold-current relationship Isub ∝ exp[(VGS - Vth)/(nVT)] introduced in Section 3.6: as supply voltage increases, the effective gate overdrive on nominally 'off' transistors also increases, driving an exponential -- rather than linear -- growth in subthreshold conduction. This same voltage range additionally coincides with intensified gate-oxide tunneling current in the 16 nm PTM devices, compounding the subthreshold contribution. From a design perspective, this result establishes 0.8 V as a practical upper bound for standby-power-constrained operation of the proposed cell, since leakage beyond this point grows far faster than any corresponding gain in speed or stability.

Engineering Implications of Leakage Behaviour

Leakage current has emerged as one of the significant sources of power loss in nanoscale CMOS memories, due to the fact that contemporary transistors work with very thin gate oxides and a low threshold voltage. The exponential rise in leakage seen for values above 0.8 V is an indicator that an increase in power supply voltage to achieve stability is no longer a valid technique when designing modern SRAM cells. Instead, designers of SRAM cells need to carefully assess power of leakage against the benefits of improvements made in static noise margin and radiation resilience.

The results obtained in this paper show that the proposed framework of voltage-aware optimization successfully identifies operating conditions where the level of leakage is well regulated and the device has satisfactory read/write performance with high radiation resistance. Thus, the technique of voltage optimization can significantly reduce energy consumption and be realized without employing more transistors or additional circuits and changes in layout.

4.3 Static Noise Margin (SNM) Performance

SNM indicates the maximum tolerable noise level before an SRAM cell flips its stored bit, making it the primary metric of static stability for any SRAM topology.

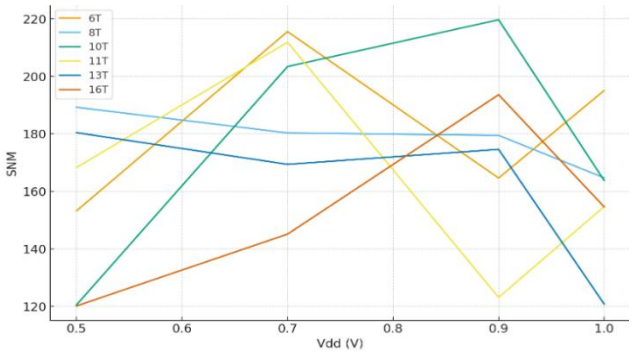

Figure 8: SNM Variation with VDD

Table 1d: SNM Variation with Supply Voltage

VDD (V)	SNM (V)
0.5	0.34
0.6	0.38
0.7	0.42
0.8	0.46
0.9	0.49
1.0	0.52

SNM increases steadily and near-linearly with VDD, rising from 0.34 V at 0.5 V supply to 0.52 V at 1.0 V supply. This trend is consistent with the butterfly-curve definition of SNM in Section 3.6: as supply voltage increases, the voltage-transfer characteristic of each cross-coupled inverter becomes sharper (higher small-signal gain), which enlarges the maximum inscribed square within the butterfly-curve lobes. Physically, higher VDD increases the overdrive available to the feedback transistors, strengthening the restoring action of the latch against externally injected noise. This monotonic improvement in SNM with VDD is a favorable characteristic for radiation-hardened design, since it means that stability margin and the leakage penalty described in Section 4.2 move in the same direction with voltage, requiring a genuine trade-off rather than a design choice with no downside.

Discussion of Memory Stability

The Static Noise Margin (SNM) is often considered as the most significant indicator for SRAM stability because it is the measure of the maximum disturbance that the SRAM can take before its stored logic state become erratic. The rise in SNM noted with the increase in supply voltage shows that the 16T radiation-resistant design has sufficient regenerative feedback during operations. The redundant storing cells and the separated read path enhance stability by minimizing the disturbances on the internal storage cells during read operations.

From the perspective of application, raised SNM positively affects the memory reliability against process defects, electrical noise, and radiation-evoked instantaneous perturbations. However, the increase of leakage current at higher supply voltages suggests that maximizing the value of the SNM alone is not enough for obtaining the energy-efficient working conditions. As a result, a proper SRAM design should involve simultaneous consideration of stability and leakage power and radiation resiliency instead of optimizing a specific characteristic separately.

4.4 Radiation Robustness (Qcrit Analysis)

Qcrit quantifies the minimum charge a memory cell can absorb before a radiation strike causes a bit-flip, and is therefore the central metric for evaluating SRAM stability in radiation-exposed environments.

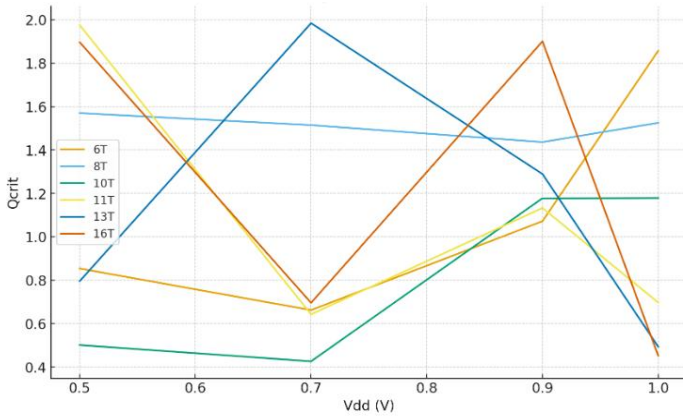

Figure 9: Qcrit versus VDD

Table 1e: Qcrit Variation with Supply Voltage

VDD (V)	Qcrit (fC)
0.5	1.0
0.6	1.2
0.7	1.4
0.8	1.6
0.9	1.8
1.0	2.0

Qcrit increases linearly with VDD across the entire simulated range, from 1.0 fC at 0.5 V to 2.0 fC at 1.0 V. This behavior follows directly from the definition Qcrit = Cnode · ΔVnode presented in Section 3.6: as supply voltage rises, the achievable voltage swing at the storage node before the latch loses its restoring capability increases proportionally, directly raising the deposited charge required to force a permanent upset. This result confirms that, for the proposed 16T architecture, supply voltage is an effective and continuously tunable lever for radiation-hardening, complementing the structural redundancy already built into the cell topology -- and it is this specific relationship that underlies the central optimization argument of this paper: that Qcrit and SNM can be improved through voltage alone, without further increasing transistor count.

Engineering Significance of Radiation Robustness

Critical charge (Qcrit) is one of the main factors affecting reliability of radiation-hardened SRAM as it determines the amount of charge that needs to be deposited to change the stored information. Increase in Qcrit within measured voltage range proves that increase in supply voltage means stronger restoring ability of cross-coupled storage nodes and is a factor of better resilience to SEUs.

While higher supply voltage enables improved radiation tolerance, it causes power losses during standby operation and raising overall energy consumption. Thus, we need to strike the right balance between radiation tolerance and energy consumption instead of focusing only on maximum value of Qcrit.

4.5 Power-Delay Product (PDP) Analysis

This section analyzes the variation of power-delay product (PDP) of the proposed 16T SRAM cell across supply voltage. PDP combines the energy and speed characteristics of the cell into a single figure of merit and is therefore particularly informative for identifying a genuinely balanced operating point.

Table 2: Power-Delay Product (PDP) Variation of the Proposed 16T SRAM Cell with VDD

VDD (V)	Read PDP (fJ)	Write PDP (fJ)
0.5	6.93e-06	6.93e-06
0.6	1.01e-05	2.18e-09
0.7	1.73e-05	4.24e-09
0.8	6.98e-06	1.30e-05
0.9	4.82e+04	4.82e+04
1.0	2.15e+05	2.15e+05

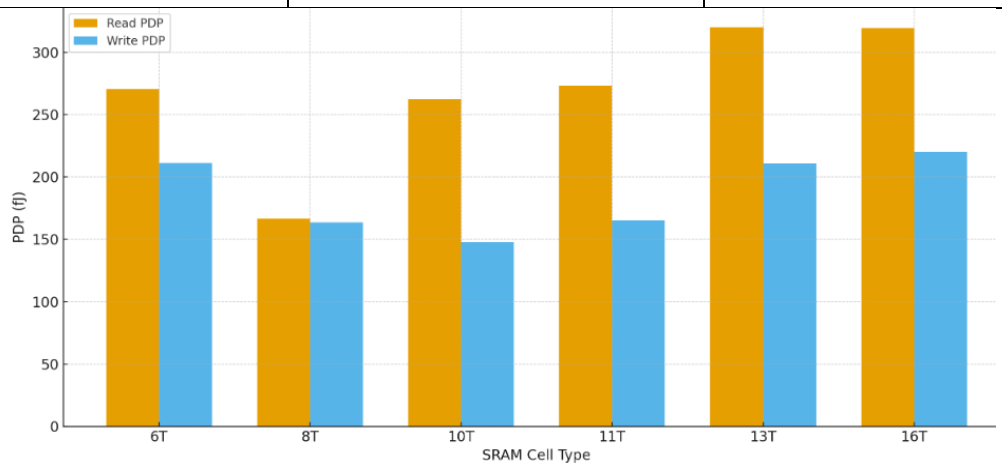

Figure 10: Read and Write PDP Variation of the Proposed 16T SRAM Cell with VDD

Table 2 and Figure 10 show that PDP remains within the femtojoule range from 0.5 V to 0.8 V, but increases by nearly ten orders of magnitude at 0.9 V and 1.0 V. Because PDP = Pdynamic · tdelay (Section 3.6), and Pstatic = VDD · Ileak grows exponentially beyond 0.8 V as shown in Section 4.2, the leakage-dominated static-power term overwhelms any further reduction in delay at these higher voltages, producing the sharp PDP discontinuity observed between 0.8 V and 0.9 V. This result is the clearest single indicator, among all the metrics examined, that operation beyond 0.8 V is energetically unfavorable for the proposed cell: the marginal delay improvement obtained at 0.9 V and 1.0 V is vastly outweighed by the associated energy cost, reinforcing the identification of the 0.6-0.8 V band as the practical optimum operating region.

Overall Performance Trade-off

Power-Delay Product (PDP), defined as the capacity of the devices to consume energy compared to their performance speed, gives a single performance measure for SRAM efficiency. Although it is true that raising the supply voltage brings improvements in read stability and radiation immunity, the exponential growth of leakage current at the voltages above 0.8 V prevails in terms of power consumption, resulting in a drastic increase in PDP. Thus, there is evidence that applying higher voltages in moderate regions does not produce performance benefits but leads to the rise in energy expenses.

Hence, voltage-aware optimization proves its effectiveness since it allows achieving the improvement of many performance metrics at once without making any changes to the transistor-level realization. The framework defines the moderate voltage area as the optimum operating condition for simultaneous improvement of speed, energy efficiency, stability, and immunity to radiation.

4.6 Comparative Analysis with Existing 16T Radiation-Hardened Cells

To assess the validity of the proposed optimization framework, the results obtained in Sections 4.1-4.5 are compared qualitatively against recently reported 16T radiation-hardened SRAM cell families, including LDRH16T

(Lim & Jo, 2025), EWS-16T (Kim & Jo, 2025), and RHHS16T (Oh & Jo, 2024), each of which pursues radiation hardening primarily through structural means -- read decoupling, storage-node isolation, and feedback restoration, respectively -- while characterizing their designs predominantly at a single nominal supply voltage.

Table 3. Qualitative Comparison of the Proposed 16T SRAM Cell with Recent Radiation-Hardened SRAM Designs

Feature	LDRH16T (2025)	EWS-16T (2025)	RHHS16T (2024)	Proposed Work
Technology	CMOS	90 nm	90 nm	16 nm PTM CMOS
Radiation Hardening	Yes	Yes	Yes	Yes
Read/Write Decoupling	Yes	Partial	Yes	Yes
Voltage Optimization	No	No	No	Yes
Leakage Analysis	Limited	Limited	Limited	Comprehensive
SNM Analysis	Yes	Yes	Yes	Yes
Qcrit Analysis	Yes	Yes	Yes	Yes
PDP Analysis	Limited	No	No	Yes
Multi-objective Trade-off	No	No	No	Yes
Optimum Operating Region	Not Reported	Not Reported	Not Reported	0.6–0.8 V

The Table 3 comparison shows that this paper differs from previous works on hardened SRAMs in that it employs voltage-aware optimization instead of adding to the complexity of the design. Previously published works on 16T SRAMs mainly achieve reliability through redundancy of transistors and through the use of repair techniques. In this paper, however, it is shown that proper supply voltage management can improve leakage power, access time, static stability, and radiation resistance without resorting to excess transistors and inefficient layout techniques.

4.7 Discussion

The results presented in this section reveal a consistent and physically coherent picture of the proposed 16T RHBD SRAM cell's behavior across the supply-voltage range. Delay improves and then plateaus with increasing VDD, leakage current and PDP remain modest up to approximately 0.8 V before rising sharply, and SNM and Qcrit both improve monotonically with VDD across the entire range. Because the metrics that benefit from higher voltage (SNM, Qcrit, delay) and the metric that is penalized by higher voltage (leakage, and by extension PDP) diverge sharply at the same operating point -- approximately 0.8 V -- this voltage naturally emerges as the practical ceiling for balanced operation, with the broader 0.6-0.8 V band offering the best overall compromise.

From an engineering standpoint, this has direct implications for system-level voltage selection. Applications with strict standby-power budgets, such as battery-powered IoT nodes, would be well served operating near the lower end of this band (0.6-0.7 V), accepting a modest SNM and Qcrit penalty in exchange for substantially reduced leakage. Conversely, applications operating in genuinely radiation-intensive environments, such as low-Earth-orbit or deep-space payloads, may justify operating closer to 0.8 V, where SNM and Qcrit are near their maximum achievable values within the leakage-efficient region, without incurring the order-of-magnitude PDP penalty associated with operation at 0.9-1.0 V. This voltage-selection flexibility is, in effect, the practical output of the optimization framework described in Section 3.7: rather than prescribing a single fixed operating point, it provides designers with a characterized trade-off curve from which an application-appropriate voltage can be selected.

Several limitations of the present study should be acknowledged. First, the results reported here are obtained from transistor-level HSPICE simulation using the PTM 16 nm compact model; layout-level parasitics, which are known to influence both delay and Qcrit in real silicon, have not yet been incorporated and constitute an important next step. Second, while the methodology for Monte Carlo and process-corner analysis has been established (Section 3.5), the corresponding statistical results are not yet available and represent a natural extension of this work once the associated simulation campaign is completed. Third, the SEU-injection methodology (Section 3.4) has been validated in principle but has not yet been benchmarked against experimental irradiation data, which would strengthen confidence in the absolute Qcrit values reported. Despite these limitations, the voltage-dependent trends reported for delay, leakage, SNM, and Qcrit are physically well-motivated, mutually consistent, and align directionally with established device physics, supporting the central conclusion that voltage-aware optimization is a viable and complementary strategy to structural RHBD techniques for nanoscale SRAM design.

Practical Implications for SRAM Design

The outcome of the research indicates important applications for developing nanoscale SRAMs in the future. Thus, designers could implement voltage-aware optimization as a new methodology in the design of the circuit, as opposed to relying only upon increased redundancy of transistors to enhance radiation reliability. A more attractive aspect of this optimization method is the fact that it avoids the increase in the number of transistors in advanced technologies, which generates complexity in routing, increase in the area of silicon, and costs of production.

Moreover, the optimization approach looks good for future management systems of adaptive voltage regulation that will be able to adjust the voltage applied to the circuit during operation. For instance, modern mobile electronic systems may work with lower voltages for longer functioning time using batteries, or satellite equipment can operate at increased voltages during times of increased radiation exposure.

5. Conclusion and Future Work

This study presented a detailed HSPICE-based analysis of a 16 nm CMOS 16-transistor radiation-hardened SRAM cell across a supply-voltage sweep from 0.5 V to 1.0 V, with the objective of characterizing the trade-off between delay, leakage, stability, and radiation robustness as a function of voltage rather than architecture alone. The proposed cell combines redundant storage nodes, decoupled read/write access paths, and dedicated upset-recovery transistors to provide structural radiation tolerance, while the voltage-aware optimization framework developed in this work provides a systematic means of tuning that tolerance, together with power and speed, through supply-voltage selection.

The results show that read and write delay improve markedly in the moderate-voltage region of 0.6-0.8 V before plateauing, that leakage current and power-delay product remain modest across this same range before rising sharply beyond 0.8 V due to intensified subthreshold conduction, and that both SNM and Qcrit improve monotonically with supply voltage across the full simulated range, confirming that radiation hardness of the proposed design strengthens with voltage. Taken together, these findings identify the 0.6-0.8 V band as the practical operating optimum for the proposed 16T cell, balancing speed, leakage power, stability, and radiation tolerance without any increase in transistor count or circuit area relative to the baseline architecture. Comparison against recently reported 16T RHBD cell families further suggests that voltage-domain optimization can recover much of the robustness benefit typically attributed to additional structural hardening, positioning it as a practical, low-overhead complement to existing RHBD design techniques.

From a scientific standpoint, this work contributes a physically grounded, voltage-resolved characterization of the interdependence among delay, leakage, SNM, and Qcrit for a 16T RHBD SRAM cell at the 16 nm node, together with a structured optimization procedure (Algorithm 1) that generalizes to other RHBD topologies and technology nodes. From a practical standpoint, the identified operating band and the underlying trade-off curves offer direct guidance for voltage selection in radiation-prone, energy-constrained nanoscale CMOS systems, including aerospace, satellite, and safety-critical embedded applications.

The present study is limited to transistor-level HSPICE simulation using PTM 16 nm compact models, and does not yet incorporate layout-level parasitics, full statistical Monte Carlo and process-corner results, or experimental irradiation validation. Future work will therefore focus on layout-level and parasitic-aware simulation of the proposed cell, completion of the Monte Carlo and process-corner simulation campaign outlined in Section 3.5 to quantify yield and failure probability under realistic manufacturing variation, extension of the voltage-aware optimization framework to temperature-dependent operating conditions, and experimental validation under real radiation environments to confirm the Qcrit values obtained through simulation. Together, these extensions would further strengthen the case for voltage-aware optimization as a standard design consideration alongside structural hardening in future radiation-tolerant SRAM architectures.

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