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Article

AI-Assisted Multi-Objective Optimization and Adaptive Control of a Feedback-Enabled 10-nm 10T FinFET SRAM Cell

S. Kulothungan[1], J. Rangaraj[2], M. Soorya[3]

[1]Research Scholar, Department of ECE, Annamalai University, Chidambaram. kulothungann@gmail.com
[2]Assistant Professor, Department of ECE, Government College of Technology, Coimbatore. ranga.jsrd@gmail.com
[3]Lecturer, Department of Computer Technology, Dr. Dharmambal Government Polytechnic College for Women, Chennai. sooryamuruganoffl@gmail.com

Abstract: Designing nanoscale Static Random Access Memory (SRAM) requires balancing power consumption, access speed, stability, and reliability under device and operating variations. Conventional manual transistor sizing relies on repeated circuit simulations and designer experience. This approach becomes inefficient when numerous discrete FinFET sizing options, operating voltages, feedback conditions, and PVT corners must be considered simultaneously. Single-objective optimization is also inadequate because SRAM design requires a balanced compromise among leakage power, dynamic power, propagation delay, Power-Delay Product (PDP), SNM, and reliability. This work presents a feedback-enabled 10T FinFET SRAM at the 10 nm technology node, integrated with a two-stage AI-based optimization framework. Non-dominated Sorting Genetic Algorithm II (NSGA-II) performs design-time multi-objective optimization of transistor configuration, supply voltage, threshold-voltage selection, and feedback strength by considering power, delay, leakage, Power-Delay Product (PDP), and Static Noise Margin (SNM). A reinforcement-learning controller subsequently adjusts the feedback condition according to write, read, hold, and adverse operating states. The SRAM is evaluated using transistor-level HSPICE simulations, Process Voltage Temperature (PVT) analysis, and Monte Carlo variation analysis. Compared with the unoptimized 10T configuration, the NSGA-II–RL design reduces write and read power by approximately 11.62% and 11.95%, respectively, while reducing the corresponding delays by 6.97% and 6.49%. Write and read PDP are reduced by approximately 17.77% and 17.67%, leakage power decreases by 19.09%, and hold SNM improves by 8.65%. The results demonstrate that combining feedback-assisted restoration with multi-objective optimization and adaptive learning provides an effective approach for improving the energy efficiency, speed, stability, and reliability of nanoscale FinFET SRAM.

Keywords: 10T SRAM, FinFET, 10-nm technology, Feedback-assisted SRAM, Adaptive feedback control, NSGA-II, Reinforcement Learning, Static Noise Margin, Power-Delay Product, PVT variation, SRAM reliability

1. INTRODUCTION

Technology scaling has increased integration density and circuit performance but has also introduced significant SRAM design challenges. FinFET-based SRAM has been widely investigated for nanoscale, low-power memory due to its improved electrostatic control [1], [2]. However, process variation, leakage current, parasitic effects, supply-voltage fluctuations, and device mismatch degrade static noise margin (SNM), write ability, power efficiency, and access speed at advanced nodes [3], [7], [16], making the trade-off among power, delay, stability, and reliability a major design challenge.

To address these limitations, higher-transistor-count architectures 8T, 9T, 10T, and 12T have been investigated to overcome the read-disturbance and stability limits of conventional 6T SRAM [4]-[10]. 10T FinFET SRAM in particular has demonstrated stable, energy-efficient operation at low supply voltages [8], [21]-[23], including for

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embedded, IoT, and wearable applications [9]-[12]. Yet transistor sizing and feedback strength strongly influence the power, delay, leakage - stability trade-off, and process-induced variation further reduces the robustness of any fixed design [16]. Evolutionary optimization has been applied to low-voltage, wide-temperature SRAM operation [19], and machine-learning techniques have been used to predict SRAM performance under process variation [20] - but to the best of our knowledge, no existing work combines Pareto-based design-time optimization with runtime, reinforcement-learning-based adaptive feedback control for a feedback-assisted FinFET SRAM. This is the gap the present work addresses.

The previous work established a feedback-enabled, restorable 10T FinFET SRAM at the 10-nm node, using a cross-coupled storage structure, controlled access devices, a dedicated read path, and a feedback-assisted restoration mechanism that recovers a degraded storage-node voltage after read disturbance or transient degradation. This work retains that architecture unchanged as its hardware foundation, since a fixed transistor configuration and feedback condition cannot be simultaneously optimal across all operating conditions stronger feedback improves stability and restoration but can raise power or hinder write operation, while aggressive sizing improves speed at the cost of leakage. This is inherently a multi-objective problem spanning power, delay, PDP, leakage, and SNM.

Accordingly, this work applies Non-dominated Sorting Genetic Algorithm II (NSGA-II) to identify Pareto-optimal configurations of the established 10T SRAM, rather than optimizing a single parameter. Because design-time optimization alone cannot address SRAM's dynamic behavior — the appropriate feedback condition differs across read, write, and hold operations, and shifts further with voltage, temperature, and process variation this work also incorporates a reinforcement-learning (RL)-based adaptive feedback controller that learns an operating-state-dependent feedback policy, reducing feedback during writes to ease data transition and strengthening it during read and hold to improve stability and recovery.

The scope of this work is to enhance the established 10T feedback-assisted FinFET SRAM at the 10-nm node without altering its transistor topology through Pareto-based NSGA-II optimization combined with RL-based adaptive feedback control, aiming for balanced improvement in energy efficiency, speed, stability, and reliability for nanoscale embedded memory.

The main contributions of this work are summarized as follows:

1. A Pareto-based NSGA-II framework that jointly optimizes power, delay, PDP, leakage, and SNM for the established 10-nm 10T feedback-assisted FinFET SRAM, without modifying its transistor topology.
2. A reinforcement-learning-based adaptive feedback controller that learns a state-dependent feedback policy across read, write, and hold operations, and under varying voltage, temperature, and process conditions.
3. An integrated two-stage framework combining design-time multi-objective optimization with runtime adaptive control, evaluated through SPICE simulation, PVT-corner analysis, and Monte Carlo reliability assessment.
4. A demonstrated, simultaneous improvement in power, delay, PDP, leakage, and stability over the unoptimized baseline design, validated for statistical robustness.

2. Literature Survey

Darji et al. proposed a sub-threshold 10T FinFET single-ended SRAM cell for energy-efficient, high-speed operation, demonstrating improved stability and reduced leakage at low voltage. The optimization remained purely architectural, without intelligent multi-objective optimization or adaptive feedback control [21].

Jali et al. introduced a subthreshold SRAM with dynamic feedback cut-off — disconnecting the feedback path during writes to improve speed and half-select immunity, restoring it otherwise for stability. This behavior is fixed by circuit-level design rather than learned, with no NSGA-II or reinforcement-learning integration [23].

Zheng et al. proposed a CNN-informed NSGA-II framework identifying Pareto-optimal 6T SRAM configurations accounting for power, timing, stability, and parasitic resistance. The study did not extend to a 10T FinFET architecture or adaptive/RL-based feedback control [24].

Zhu et al. developed an RL-driven optimization framework for CMOS 8T SRAM, automating power–delay–area trade-offs without manual parameter selection. Adaptive feedback control and reliability-aware operation for a 10T FinFET SRAM were not addressed [25].

Kao et al. proposed a PVT-resilient subthreshold SRAM in-memory-computing accelerator with in-situ regulation for reliable operation across process, voltage, and temperature. The work targets in-memory computing rather than adaptive feedback control, and does not combine PVT regulation with NSGA-II and RL [26].

Shahin et al. examined SRAM reliability beyond 3 nm under design-time and run-time variability in CFET technology, showing reliable operation requires both. No learning-based feedback mechanism for 10T FinFET SRAM was proposed, nor were NSGA-II and RL jointly employed [27].

Deshwal et al. analyzed aging, self-heating, and parasitic effects in NSFET/CFET devices, highlighting reliability concerns for SRAM power, delay, stability, and retention. No intelligent feedback-control mechanism or NSGA-II/RL-based compensation was proposed [28].

Peng et al. proposed MOIL, a multi-objective SRAM optimization framework using incremental learning to explore conflicting power–delay–area–stability requirements. It does not target a 10T FinFET architecture or combine NSGA-II with RL-based feedback adaptation [30].

Nii and Kobayashi proposed an energy-efficient dual-port 8T SRAM with a disturbance-aware, self-adjustable replica-tracking circuit improving read/write robustness. Adaptation relies on a dedicated tracking circuit, not a learning-based mechanism, with no NSGA-II or RL [31].

Sharma et al. proposed a FinFET-based low-power write-enhanced SRAM using a write-assist mechanism to improve stability and write reliability at low voltage. The design uses predefined circuit parameters, without intelligent optimization or PVT-aware adaptive feedback control [33].

Pilo et al. proposed a high-density SRAM in Intel 18A technology using a resistive supply-line write scheme with parallel-boost write-assist circuitry. The work focuses on physical implementation rather than intelligent adaptive optimization, with no NSGA-II, RL, or adaptive feedback control [35].

2.1 Research Gap and Motivation

Despite extensive research on FinFET-based SRAM architectures, achieving a balanced trade-off among power, delay, leakage, and stability remains challenging at nanoscale nodes. Existing 8T, 9T, 10T, and 12T designs primarily target individual characteristics read stability, write ability, or low-power operation while process, voltage, and temperature variations continue to affect fixed configurations. Evolutionary algorithms have been applied to SRAM design, but comprehensive Pareto-based optimization across multiple conflicting objectives remains limited; separately, conventional feedback mechanisms remain fixed and cannot adapt across read, write, and hold conditions excessive feedback raises power or degrades write ability, while insufficient feedback weakens data restoration. To the best of our knowledge, no existing work jointly combines Pareto-based multi-objective optimization with reinforcement-learning-based adaptive feedback control for a 10T FinFET SRAM. Motivated by this, the present work retains the 10T FinFET SRAM architecture at the 10-nm node and integrates NSGA-II-based multi-objective optimization with an RL-based adaptive feedback controller, aiming for an improved trade-off among power, delay, PDP, leakage, SNM, and reliability under varying operating conditions.

Based on the identified research gaps and the above motivation, the proposed work develops an optimized 10-nm 10T FinFET SRAM framework that combines Pareto-based NSGA-II multi-objective optimization with reinforcement-learning-based adaptive feedback control, as detailed in the following section.

3. Overall Proposed Framework

The proposed methodology develops an optimized and adaptive 10T FinFET SRAM architecture at the 10-nm technology node by integrating feedback-assisted data restoration, Pareto-based multi-objective optimization, and reinforcement-learning-based adaptive feedback control. The complete framework consists of sequential stages, beginning with 10-nm FinFET device characterization and proceeding through 10T SRAM design, functional analysis, PVT variation modeling, NSGA-II optimization, Pareto-optimal solution selection, RL-based adaptive feedback control, SPICE validation, and Monte Carlo reliability analysis. The overall workflow of the proposed methodology is illustrated in Figure 1.

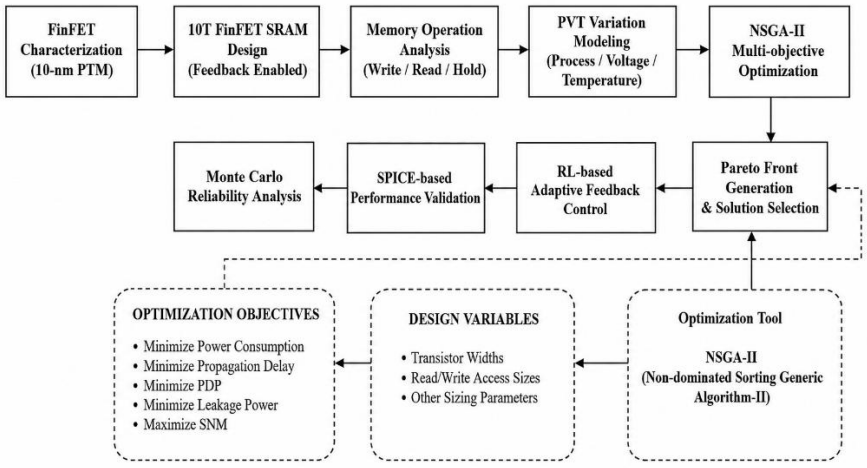


Figure 1. Overall proposed methodology and optimization framework.

As shown in Figure 1, the methodology initially characterizes the 10-nm FinFET device using the Predictive Technology Model (PTM) and Synopsys HSPICE. The characterized device is then used to construct the proposed 10T FinFET SRAM incorporating a feedback-assisted restoration mechanism. The designed cell is evaluated under write, read, and hold operations to verify its functional behavior.

Following functional verification, process, voltage, and temperature (PVT) variations are incorporated to examine the sensitivity of the SRAM to operating and device-level variations. The resulting power, delay, leakage, and stability characteristics are supplied to the optimization stage. The NSGA-II algorithm then performs multi-objective design-space exploration by simultaneously considering power consumption, delay, PDP, leakage power, and SNM. Through non-dominated sorting and crowding-distance-based selection, NSGA-II generates a set of Pareto-optimal SRAM configurations, from which an appropriate compromise solution is selected. The selected optimized configuration is subsequently provided to the reinforcement-learning-based adaptive feedback controller. The controller observes the operating state and relevant electrical conditions and determines an appropriate feedback action for different SRAM modes. This enables the feedback mechanism to adapt during write, read, and hold operations instead of relying on a fixed feedback condition.

Finally, the optimized and adaptively controlled SRAM is validated using SPICE-based transient, DC, power, leakage, delay, and SNM analyses. Statistical robustness is further investigated using Monte Carlo simulation, where device and process variations are introduced and the resulting distributions of SNM, power, delay, and leakage are evaluated using statistical measures and yield. Thus, the proposed framework establishes a systematic progression from 10-nm FinFET device characterization → 10T SRAM design → functional analysis → PVT modeling → Pareto-based NSGA-II optimization → optimized configuration selection → RL-based adaptive feedback control → SPICE validation → Monte Carlo reliability analysis. This integrated methodology

provides the foundation for the detailed circuit architecture and optimization procedures presented in the following subsections.

3.1 FinFET Transistor Characterization

FinFET technology is selected because its three-dimensional fin structure provides improved electrostatic control over the conducting channel compared with conventional planar MOSFETs. The gate surrounds the fin channel, thereby reducing short-channel effects and improving control over the threshold voltage and leakage current. These characteristics make FinFET devices suitable for low-power SRAM applications.

However, continued technology scaling to the 10nm node introduces variations in important electrical parameters such as threshold voltage V_{TH}, drain current, leakage current, fin dimensions, gate length, and oxide thickness. Such variations can affect SRAM stability, power consumption, delay, and memory yield.

The principal transistor characteristics considered in this work are the ON-current I_{ON}, OFF-current I_{OFF}, threshold voltage V_{TH}, and subthreshold leakage current. The ON/OFF current ratio and subthreshold leakage characteristics are used to assess the switching capability and leakage behavior of the 10-nm FinFET device. The corresponding expressions are retained from the existing methodology. The ON/OFF current ratio is expressed as

$$R_{ON/OFF} = \frac{I_{ON}}{I_{OFF}} \quad (1)$$

where I_{ON} represents the current when the FinFET is in the conducting state and I_{OFF} represents the leakage current when the device is switched OFF.

The subthreshold leakage current can be approximately represented as

$$I_{sub} = I_0 exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right) \quad (2)$$

where I_0 is the reference current, n is the subthreshold slope factor, and V_T is the thermal voltage.

The characterized FinFET parameters provide the required device-level information for constructing and evaluating the proposed 10T FinFET SRAM at the 10-nm technology node. These characteristics are subsequently used in the SRAM functional analysis, PVT variation assessment, multi-objective optimization, and reliability evaluation.

3.2 10T FinFET SRAM Architecture

The proposed SRAM cell consists of 10 FinFET transistors (M1–M10) and is designed for low-power and stable memory operation. The architecture retains the feedback-assisted structure of the original design while adopting the 10-nm FinFET technology. The overall transistor configuration is maintained so that Work 3 represents an updated version of the existing SRAM architecture with the technology node revised to 10 nm. The cross-coupled transistors form the primary storage latch and maintain complementary logic states at the internal storage nodes Q and QB. The access transistors provide controlled interaction between the storage nodes and the complementary bit lines during write operations. A dedicated read path is employed for data sensing while reducing direct disturbance to the internal storage nodes. The feedback transistors provide an additional restoration path that reinforces the stored logic state when the voltage of an internal storage node is degraded during circuit operation. The transistor-level structure of the proposed 10T FinFET SRAM cell is illustrated in Figure 2.

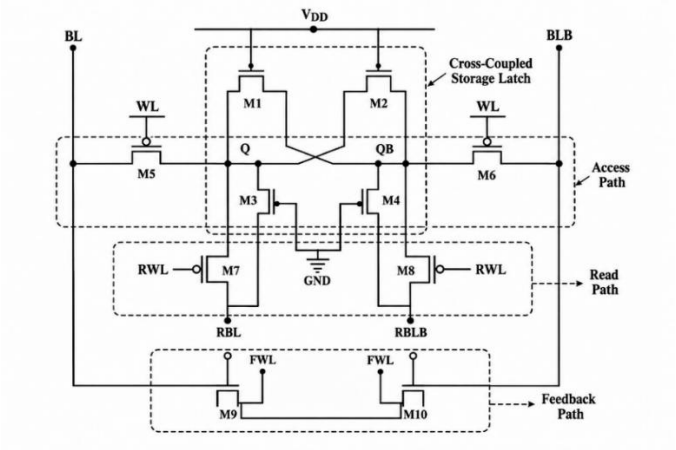


Figure 2. Proposed 10T FinFET SRAM architecture at the 10-nm technology node

The cross-coupled storage structure maintains the stored data during the hold operation, whereas the access devices enable controlled data transfer during the write operation. The dedicated read path minimizes the direct loading of the storage nodes during data sensing. In addition, the feedback mechanism assists in restoring the disturbed storage node and thereby improves the robustness of the stored data. The resulting 10T architecture provides the circuit-level foundation for the subsequent PVT analysis, Pareto-based multi-objective optimization, adaptive feedback control, and reliability evaluation.

3.2.1 Memory Write Operation

During the write operation, complementary data are applied to BL and BLB. The word line is activated to enable the access transistors. The applied bit-line values overcome the existing state of the cross-coupled storage latch and establish the new data state at Q and QB.

The write operation requires the feedback path to be sufficiently weakened to allow the external write signal to overwrite the previously stored information. Therefore, feedback strength becomes an important design parameter affecting write ability and write delay.

The write delay is expressed as

$$T_{write} = t_{Q,new} - t_{WL} \quad (3)$$

Where $t_{Q,new}$is the time at which the storage node reaches the required new logic state and t_{WL} represents the word-line activation time.

3.2.2 Memory Read Operation

Before a read operation, the bit lines are precharged according to the selected read scheme. The word line is then activated, enabling the dedicated read transistors. The read path is electrically separated from the internal storage nodes to reduce the possibility of read disturbance. Depending on the stored data, the corresponding read path produces a voltage difference at the bit line, which is sensed by the external read circuitry. The read stability of the SRAM is evaluated using the Static Noise Margin (SNM). The SNM can be obtained from the voltage transfer characteristics of the cross-coupled inverters using the conventional butterfly-curve method. A higher SNM indicates improved immunity against noise-induced data flipping.

3.2.3 Feedback-Control Operation

The feedback path is the central control mechanism of the proposed architecture. During the hold operation, sufficient feedback is maintained to preserve the stored data. During read operation, the feedback is controlled to

improve stability and prevent disturbance. During write operation, the feedback is weakened to facilitate data overwriting. Therefore, the feedback control problem can be expressed as

$$F(t) = f(V_{DD}, T, V_{TH}, SNM, P_{LEAK}, T_{delay}, Mode) \quad (4)$$

where F(t) represents the feedback-control condition and Mode represents the current SRAM operating mode. The proposed architecture employs an adaptive feedback-control mechanism in which the feedback condition is determined according to the observed operating state. This feedback-control strategy is subsequently integrated with the proposed NSGA-II-based multi-objective optimization and reinforcement-learning framework to determine suitable feedback conditions under different operating conditions.

3.3 PVT Variation and Corner-Based Reliability Modeling

The performance of the 10T FinFET SRAM at the 10-nm technology node is evaluated under Process–Voltage–Temperature (PVT) variations to account for deterministic changes in fabrication conditions, supply voltage, and operating temperature. Process variation is represented using predefined process corners such as typical–typical (TT), fast–fast (FF), slow–slow (SS), fast–slow (FS), and slow–fast (SF), while voltage variation is introduced by considering the minimum, nominal, and maximum supply-voltage conditions. Temperature variation is evaluated over the specified operating temperature range. Accordingly, each candidate SRAM configuration is evaluated across 45 PVT corners, obtained from 5 process corners (TT, FF, SS, FS, and SF), 3 supply-voltage conditions (minimum, nominal, and maximum), and 3 temperature points (−40 °C, 25 °C, and 125 °C). For each candidate SRAM configuration generated during NSGA-II optimization, SPICE simulations are performed under the selected PVT corners. The resulting leakage power, dynamic power, propagation delay, SNM, and PDP values are used to construct the PVT-aware objective functions. This enables NSGA-II to identify SRAM configurations that provide suitable trade-offs among power, speed, stability, and robustness across different deterministic operating conditions.

PVT analysis therefore represents predefined worst-case and nominal operating conditions, whereas Monte Carlo analysis is subsequently employed as a separate statistical evaluation to investigate random device variations and mismatch. The distinction between deterministic PVT analysis and statistical Monte Carlo analysis ensures that both operating-corner robustness and manufacturing-related variability are systematically evaluated.

The overall PVT condition can be represented as

$$PVT = (P, V, T) \quad (5)$$

where P represents process conditions, V represents supply voltage, and T represents temperature. The reliability-aware optimization considers the effect of these variations on leakage power, dynamic power, propagation delay, SNM, write ability, read stability, power-delay product, and data retention. During each NSGA-II generation, candidate SRAM configurations are evaluated through SPICE simulations under the predefined PVT conditions. The resulting PVT-aware power, delay, SNM, and PDP values are used to calculate the objective functions and guide the evolutionary optimization toward robust Pareto-optimal solutions.

3.4 NSGA-II-Based Multi-Objective Optimization

The first intelligent layer of the proposed framework uses the Non-dominated Sorting Genetic Algorithm II (NSGA-II) to identify optimized design parameters for the proposed 10-nm 10T FinFET SRAM. SRAM design involves conflicting objectives. For example, reducing transistor size can reduce capacitance and power but may degrade stability and increase delay. Increasing feedback strength can improve retention and SNM but can make writing more difficult.

Therefore, a single-objective optimization method is insufficient for simultaneously achieving low power, high speed, improved stability, and energy efficiency. NSGA-II is employed to obtain a set of Pareto-optimal solutions that provide different trade-offs among these conflicting objectives.

The optimization problem is formulated as

$$F(X) = [f_1(X), f_2(X), f_3(X), f_4(X), f_5(X)] \quad (6)$$

where $f_1$is the leakage power, f_2 is the dynamic power, $f_3$is the propagation delay, f_4 is the inverse SNM and $f_5$is the PDP. Then the design vector is

$$X = [W_1, W_2, \ldots . V_{DD}, V_{TH}] \quad (7)$$

and the objectives include leakage power, dynamic power, delay, SNM, and PDP.

3.4.1 Optimization Variables

The principal optimization variables include FinFET transistor dimensions, transistor sizing ratios, threshold-voltage configuration, and supply voltage. These parameters are fixed once the circuit is fabricated and therefore define the design-time search space for NSGA-II. Feedback strength is deliberately excluded from this vector: unlike transistor sizing or supply voltage, it can be adjusted during operation without requiring circuit redesign, and is instead determined at runtime by the RL-based adaptive controller described in Section 3.5. During NSGA-II evaluation, each candidate is simulated with feedback strength held at a fixed nominal baseline (Fmedium), so that all candidates are compared under identical feedback conditions; this baseline is later replaced by the RL agent's state-dependent policy once the design is finalized.

3.4.2 Objective Functions

The first objective minimizes leakage power: $f_1 = P_{leak}$ (8)

The second objective minimizes dynamic power: $f_2 = P_{dyn}$ (9)

The third objective minimizes propagation delay: $f_3 = T_{delay}$ (10)

The fourth objective maximizes SNM. Since NSGA-II is formulated as a minimization problem, SNM can be expressed as $f_4 = \frac{1}{SNM}$ (11)

The fifth objective minimizes the Power-Delay Product: $f_5 = P\ X\ T_{delay}$ (12)

Thus, the optimization simultaneously considers power, speed, stability, and energy efficiency.

3.4.3 NSGA-II Optimization Procedure

The NSGA-II optimization begins by generating an initial population of candidate configurations for the proposed 10-nm 10T FinFET SRAM. Each candidate represents a specific combination of the defined transistor sizing parameters, supply voltage, threshold-voltage configuration, and feedback strength. The candidate configurations are evaluated through SPICE simulation to obtain the corresponding leakage power, dynamic power, propagation delay, SNM, and PDP under the predefined operating conditions. These performance measures are subsequently supplied to the NSGA-II objective functions.

The candidate solutions are ranked using non-dominated sorting, in which solutions are assigned to different Pareto fronts according to their dominance relationships. A crowding-distance measure is then calculated to maintain diversity among solutions within the same front. Based on the resulting rank and crowding distance, suitable parent solutions are selected and genetic crossover and mutation operations are applied to generate new candidate configurations. The new population is subsequently evaluated through SPICE and compared with the preceding population. This evolutionary process is repeated until the specified convergence or stopping criterion is satisfied.

The optimization process generates a set of non-dominated Pareto-optimal solutions rather than a single solution, thereby providing different trade-offs among power consumption, propagation delay, SNM, and PDP. The resulting Pareto front is subsequently analyzed to select the most appropriate configuration for the proposed SRAM. The selected configuration is then used as the optimized baseline for the reinforcement-learning-based adaptive feedback controller.

3.4.4 Pareto-Optimal Solution Selection

A solution X_a dominates another solution X_b when X_a is no worse than X_b for all objectives and is strictly better for at least one objective. The resulting Pareto front provides different trade-offs between power, delay, SNM, and PDP. A final solution can be selected according to a normalized decision score:

$$S_i = \sum_{j=1}^{m} \quad w_j f_{ij} \tag{13}$$

where w_j represents the importance assigned to objective j. The selected Pareto solution becomes the optimized baseline for the subsequent RL-based adaptive feedback controller.

3.5 Reinforcement-Learning-Based Adaptive Feedback Control

NSGA-II provides optimized design parameters for the proposed 10-nm 10T FinFET SRAM, but it does not continuously adapt the feedback condition during changing operating conditions. Therefore, the second intelligent layer employs Reinforcement Learning (RL) to provide adaptive feedback control. The RL controller interacts with the SRAM operating environment and learns which feedback-control action provides the best performance for a particular operating state. The RL framework consists of: Agent → SRAM Environment → State → Action → Reward → Next State

3.5.1 State Definition

The state vector represents the current operating and reliability condition of the SRAM. The state includes the operating mode together with the relevant electrical and reliability parameters used by the controller.

$$S_t = [V_{DD}, T, V_{TH}, P_{leak}, T_{delay}, SNM, Mode] \tag{14}$$

where *Mode* represents read, write, or hold operation. The state therefore provides the RL agent with information regarding both circuit performance and reliability.

3.5.2 Action Definition

The action represents the feedback-control decision made by the RL agent. The controller selects a feedback-strength condition based on the complete observed state vector *St*, rather than on the operating mode alone. For example,

$$At \in \{F_{low}, F_{medium}, F_{high}\} \tag{15}$$

where F_{low} represents weak feedback, F_{medium} represents moderate feedback, and F_{high} represents strong feedback. The operating mode establishes a baseline feedback tendency: weaker feedback during write operation to facilitate data overwriting, an intermediate condition during read operation to improve stability while limiting disturbance, and stronger feedback during hold operation to improve data retention. However, the final action is not determined by mode alone. Within a given mode, the agent escalates toward F_{high} when the observed temperature *T*, threshold-voltage deviation *VTH*, or static noise margin *SNM* indicate degraded stability margins, and relaxes toward F_{low} or F_{medium} when these indicators reflect favorable operating conditions. For instance, a hold operation evaluated at nominal temperature and SNM is assigned F_{medium}, whereas the same hold operation under high temperature or a reduced SNM is escalated to F_{high}. This state-dependent behavior allows a single operating mode to receive different feedback actions depending on the prevailing electrical and reliability conditions, distinguishing the learned policy from a fixed, mode-only lookup rule.

3.5.3 Reward Function

The reward function guides the RL agent toward feedback-control decisions that provide improved overall SRAM performance. A general reward function is formulated as

$$R_t = -w_1\tilde{P}_{leak} - w_2\tilde{P}_{dyn} - w_3\tilde{T}_{delay} + w_4\widetilde{SNM} - w_5\widetilde{PDP} - w_6R_{failure} \quad (16)$$

where $R_{failure}$represents a reliability penalty and where the tilde indicates normalized parameters. Normalization is important because power, delay, SNM and reliability penalty have different numerical scales. A higher reward is obtained when the SRAM exhibits low power, low delay, high SNM, low PDP, and reliable operation.

3.5.4 RL Training

During training, the RL agent observes the current SRAM state, selects a feedback action, receives a reward, and observes the resulting state. The state-action value can be represented as

$$Q(s_t, a_t) \leftarrow Q(s_t, a_t) + \alpha[R_t + a'\gamma Q\ (s_{t+1}, a') - Q(s_t, a_t) \quad (17)$$

where γ is the discount factor, α is the learning rate, R_t indicates the reward, s_t represents the current state, $a_t\ denotes$ the selected action, s_{t+1} is the next state. Through repeated interactions, the agent learns an optimal policy

$$\pi^*(s) = arg\ arg\ max\ a\ \ Q(s, a) \quad (18)$$

that determines the most appropriate feedback condition for a given operating state.

3.5.5 Adaptive Feedback Control

After training, the RL controller dynamically selects the feedback condition according to the observed SRAM operating state and reliability conditions. During the write operation, the feedback strength is reduced to facilitate reliable overwriting of the stored data. During the read operation, the feedback condition is adjusted to maintain high read stability while preventing data disturbance. During the hold operation, stronger feedback is applied to preserve the stored state and improve retention stability. Under high-temperature or high-variation conditions, the controller selects a reliability-oriented feedback condition to maintain stable operation under adverse conditions.

Thus, the trained RL agent provides state-dependent feedback control by continuously selecting the most suitable feedback condition according to the electrical and operating characteristics of the SRAM. This adaptive mechanism enables the proposed 10T FinFET SRAM to achieve an improved trade-off among write ability, read stability, data retention, power consumption, and reliability under varying operating conditions.

3.6 Integrated NSGA-II–RL Framework

The complete proposed framework integrates NSGA-II-based multi-objective optimization with reinforcement-learning-based adaptive feedback control to improve the performance and reliability of the proposed 10T FinFET SRAM at the 10-nm technology node. NSGA-II performs the global exploration of the SRAM design space and identifies a set of Pareto-optimal configurations, whereas the trained RL agent performs state-dependent feedback-control decisions under different operating conditions. The overall workflow is therefore expressed as 10T FinFET SRAM → PVT Modeling → NSGA-II Optimization → Pareto-Optimal Solution → RL Training → Adaptive Feedback Control → Reliability Validation.

The optimized transistor parameters obtained from NSGA-II are first applied to the SRAM circuit, and the resulting optimized circuit is used as the environment for RL training. The RL agent observes the operating and reliability state of the SRAM and learns an appropriate feedback-control policy through repeated interaction with the circuit environment. In this way, NSGA-II determines a globally optimized circuit configuration, while RL dynamically adjusts the feedback condition according to the instantaneous operating requirements.

This two-level strategy avoids applying reinforcement learning directly to the complete SRAM design space, which can result in a large computational search space. Instead, NSGA-II first narrows the design space to high-quality Pareto-optimal configurations, after which RL concentrates on adaptive feedback control. The integrated framework consequently combines global multi-objective circuit optimization with local state-dependent control, enabling

improved trade-offs among power consumption, propagation delay, SNM, PDP, write ability, read stability, data retention, and reliability.

3.7 SPICE-Based Performance Evaluation

SPICE-based circuit simulation is employed at two stages of the proposed framework. First, SPICE evaluates each candidate 10T FinFET SRAM configuration at the 10-nm technology node generated by NSGA-II under the predefined PVT conditions. The resulting dynamic power, leakage power, propagation delay, SNM, and PDP values are used as objective functions for non-dominated sorting and evolutionary optimization until the Pareto-optimal solution set is obtained. After RL-based adaptive feedback training, SPICE is used for final circuit-level validation of the optimized SRAM. Transient and DC analyses are performed to verify write, read, and hold operations, while power, leakage, delay, and SNM are evaluated under PVT and Monte Carlo variations to assess robustness and reliability. The principal performance metrics include average power, leakage power, propagation delay, PDP, energy per operation, and SNM, which are finally compared with selected SRAM architectures to demonstrate the effectiveness of the proposed framework.

Average Power

$$P_{avg} = \frac{1}{T}\int_0^T \quad V_{DD}(t)I_{DD}(t)dt \tag{19}$$

Power-Delay Product

$$PDP = P_{avg}X\,T_{delay} \tag{20}$$

Leakage Power

$$P_{leak} = V_{DD}XI_{leak} \tag{21}$$

Energy per Operation

$$E_{op} = P_{avg}X\,T_{op} \tag{22}$$

The proposed design is compared with conventional and previously reported SRAM architectures to quantify its performance improvement.

3.8 Monte Carlo Reliability Analysis

Monte Carlo analysis is employed as a statistical reliability assessment after the NSGA-II optimization and RL-based adaptive feedback control of the proposed 10T FinFET SRAM. Unlike PVT analysis, which evaluates predefined deterministic process, voltage, and temperature corners, Monte Carlo analysis introduces random variations in device and process parameters according to specified statistical distributions. This analysis is used to evaluate the sensitivity of the optimized and adaptively controlled 10-nm FinFET SRAM to manufacturing-related variations and device mismatch.

The statistical analysis considers variations in parameters such as threshold voltage, transistor mismatch, fin width, gate length, oxide-related parameters, and leakage current**.** For each Monte Carlo iteration, the selected SRAM configuration is simulated using a randomly generated set of device parameters. The resulting distributions of power, propagation delay, SNM, leakage current, and other relevant performance parameters are subsequently analyzed to determine the statistical robustness of the proposed SRAM. For the statistical reliability evaluation, 1000 Monte Carlo simulation runs are performed on the final NSGA-II–RL-optimized SRAM configuration, with a randomly generated set of device and process parameters applied in each run.

For N Monte Carlo samples, the mean performance is calculated as

$$\mu_X = \frac{1}{N}\sum_{i=1}^{N} \quad X_i \tag{23}$$

and the standard deviation is

$$\sigma_X = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N} (X_i - \mu_X)^2} \quad (24)$$

The coefficient of variation can be expressed as

$$CV = \frac{\sigma_X}{\mu_X} \quad (25)$$

A lower variation in power, delay, and SNM indicates improved robustness against random device-level variations. The statistical yield can be estimated as

$$Yield = \frac{N_{pass}}{N} X100 \quad (26)$$

where N_{pass} represents the number of Monte Carlo samples satisfying the predefined performance and reliability constraints. A lower standard deviation and coefficient of variation indicate reduced sensitivity to random parameter variations, while a higher statistical yield indicates improved manufacturing robustness. Therefore, Monte Carlo analysis provides an independent statistical validation of the final 10-nm 10T FinFET SRAM after NSGA-II optimization and RL-based adaptive feedback control. The analysis verifies whether the performance improvements obtained through the proposed framework remain consistent in the presence of random device and process variations.

3.9 Computational Optimization and Validation Framework

The framework integrates NSGA-II-based multi-objective optimization with RL-based adaptive feedback control to improve the power, delay, stability, energy efficiency, and reliability of the proposed SRAM. The computational workflow of the proposed optimization framework is illustrated in Figure 3. The process begins with the establishment of the 10T FinFET SRAM architecture and definition of the relevant design variables, operating conditions, and process-voltage-temperature (PVT) variations. An initial population of candidate solutions is then generated for the NSGA-II-based multi-objective optimization. Each candidate configuration is evaluated through SPICE simulation using power consumption, propagation delay, static noise margin (SNM), leakage power, and power-delay product (PDP) as the principal performance objectives. Through non-dominated sorting, crowding-distance evaluation, selection, crossover, and mutation, the candidate population is iteratively evolved toward a Pareto-optimal solution set.

The selected optimized configuration is subsequently used as the environment for the reinforcement learning (RL) stage. The RL agent observes the operating state of the SRAM and determines an appropriate feedback-control action according to the operating condition. The resulting response is evaluated using a reward formulation that considers power, delay, stability, and reliability objectives. The control policy is iteratively updated to obtain an adaptive feedback strategy for the write, read, and hold operations. Finally, the optimized and adaptively controlled SRAM configuration is validated using SPICE-based simulations together with PVT and Monte Carlo analyses. The resulting electrical and reliability characteristics are presented and discussed in Section 4.

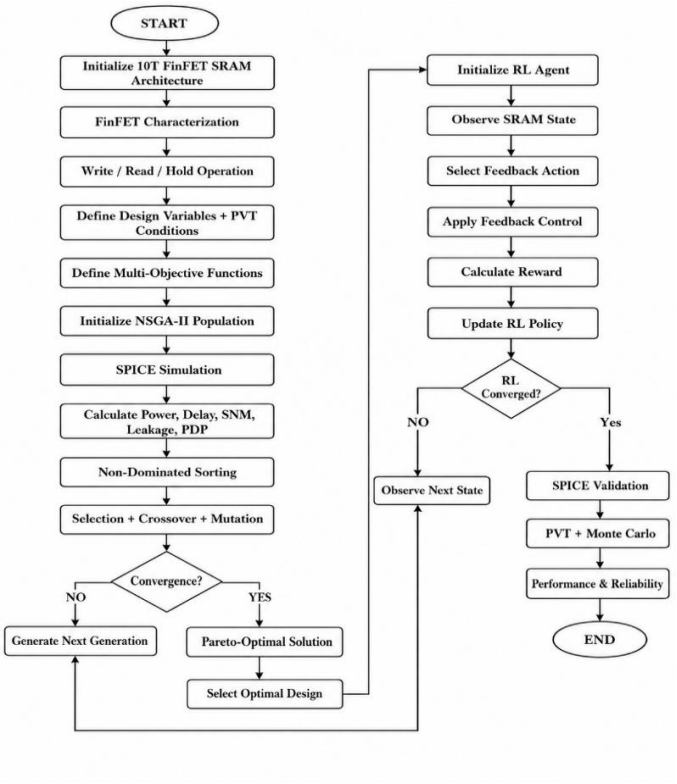


Figure 3. Computational workflow of the proposed NSGA-II and RL-based optimization framework.

4. RESULTS AND DISCUSSION

The proposed feedback-enabled restorable 10T FinFET SRAM is evaluated at the 10-nm technology node using transistor-level Synopsys HSPICE simulations. The evaluation investigates the functional correctness, power consumption, propagation delay, power-delay product (PDP), leakage characteristics, static noise margin (SNM), feedback-assisted data restoration, and overall reliability of the proposed SRAM cell. The performance analysis is further extended using the proposed NSGA-II-based multi-objective optimization and reinforcement-learning-based adaptive feedback control to investigate the trade-offs among power, speed, stability, energy efficiency, and reliability.

The results are presented through functional waveform analysis, quantitative performance evaluation, optimization results, adaptive feedback behavior, and PVT and Monte Carlo variation analyses. These evaluations provide a comprehensive assessment of the proposed 10-nm feedback-enabled restorable 10T FinFET SRAM under different operating and variation conditions.

4.1 Simulation Setup and Parameters

The proposed feedback-enabled restorable 10T FinFET SRAM is evaluated using the 10-nm FinFET Predictive Technology Model (PTM) in Synopsys HSPICE**.** Transistor-level simulations are performed to characterize the electrical and functional behavior of the proposed SRAM cell under the defined operating conditions. The evaluation considers the four principal operating conditions: hold, read, write, and feedback-assisted data restoration**.**

The simulated responses are analyzed to determine the key performance parameters, including average power consumption, read delay, write delay, power-delay product (PDP), leakage current, leakage power, static noise margin (SNM), and data-retention/restoration characteristics**.** These parameters are selected to provide a comprehensive assessment of the power efficiency, operating speed, stability, and reliability of the proposed 10-nm SRAM architecture.

In addition to the circuit-level performance evaluation, the proposed NSGA-II-based multi-objective optimization is applied to identify suitable design configurations considering the conflicting objectives of power, delay, PDP, leakage, and SNM. The optimized configuration is subsequently used by the reinforcement-learning-based adaptive feedback controller to determine an appropriate feedback condition according to the SRAM operating state. The final configuration is further evaluated using SPICE, PVT, and Monte Carlo simulations to assess its performance and robustness under deterministic and statistical variations.

4.2 Functional Verification of the 10T FinFET SRAM

The functional operation of the proposed 10-nm feedback-enabled restorable 10T FinFET SRAM is first verified through transistor-level transient simulation. The write, read, and hold operations are evaluated to confirm correct data updating, nondestructive data retrieval, and stable data retention, respectively.

4.2.1 Write Operation

During the write operation, complementary data are applied to BL and BLB while the word line is activated. The access transistors transfer the input data to the internal storage nodes Q and QB. Q and QB transition to complementary logic states corresponding to the applied data, confirming successful writing of the proposed 10-nm SRAM cell.

4.2.2 Read Operation

During the read operation, the dedicated read path is activated to sense the stored data through the read bit line. The stored information is successfully sensed while the voltage levels of Q and QB remain stable. The isolated read path reduces direct disturbance of the storage nodes during data retrieval.

4.2.3 Hold Operation

The hold operation is evaluated with the word line disabled. Q and QB maintain their complementary voltage levels throughout the hold interval, confirming stable data retention in the proposed 10-nm 10T FinFET SRAM.

4.3 NSGA-II-Based Multi-Objective Optimization Results

The proposed 10-nm 10T FinFET SRAM is optimized using the NSGA-II multi-objective optimization algorithm considering power consumption, propagation delay, SNM, leakage power, and PDP as competing objectives. Each candidate configuration is evaluated through SPICE simulation, and the resulting electrical characteristics are used to guide the evolutionary optimization process. The optimization convergence is illustrated in Figure 4. During the initial generations, the candidate solutions exhibit a wide range of performance characteristics. As the number of generations increases, dominated solutions are progressively eliminated and the population moves toward a stable Pareto-optimal region. This convergence indicates that NSGA-II effectively identifies suitable trade-offs among power, delay, stability, and energy efficiency rather than optimizing a single performance metric**.**

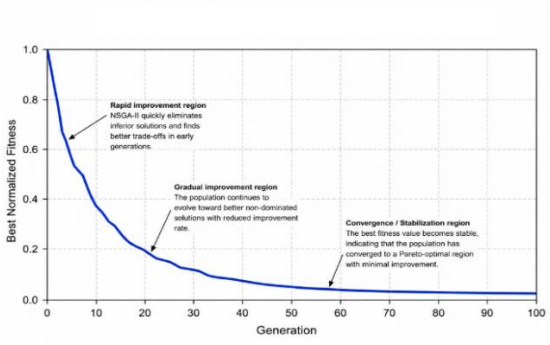


Figure 4. NSGA-II optimization convergence curve

The convergence curve is obtained from the generation-wise NSGA-II optimization process, where each population is evaluated through the defined SRAM performance objectives. For every generation, the best fitness/objective value of the non-dominated population is recorded and used to construct the convergence curve. The progressive reduction and stabilization of this value indicate that the population is approaching a stable Pareto-optimal region. The curve is terminated at the predefined convergence generation, where no significant improvement is observed.

4.3.1 Pareto-Optimal Solution Analysis

The non-dominated solutions obtained from the NSGA-II optimization are represented by the Pareto front in Figure 5. Each solution corresponds to a different trade-off among power consumption, propagation delay, stability, leakage, and PDP. The Pareto distribution demonstrates that improving one objective may adversely affect another; therefore, no single solution simultaneously provides the optimum value for all objectives. A suitable configuration is selected from the Pareto-optimal set using the normalized decision criterion defined in Section 3.

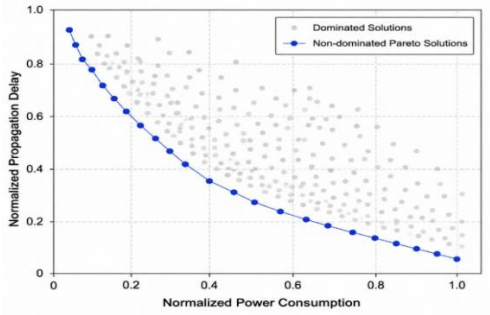


Figure 5. Pareto-optimal solutions obtained using NSGA-II.

4.4 Reinforcement-Learning-Based Adaptive Feedback Results

The NSGA-II-optimized configuration provides the design-level parameters for the SRAM, while the reinforcement-learning (RL) controller adaptively adjusts the feedback condition according to the observed operating state. During write operation, the controller reduces the feedback strength to facilitate data overwriting, whereas during read operation it adopts a stability-oriented feedback condition to preserve the stored state. Stronger feedback is maintained during hold operation to improve data retention, while reliability-oriented feedback is selected under high-temperature and high-variation conditions.

The RL training behavior is represented by the reward convergence in Figure 6. During the initial training stage, the agent explores different feedback actions, and the reward progressively improves as the controller learns suitable actions.

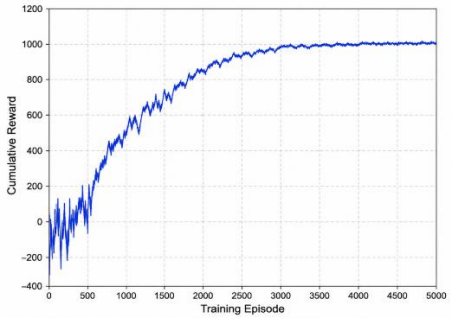


Figure 6. RL training reward and convergence curve.

4.5 PVT-Aware Performance Analysis

PVT analysis is performed to evaluate the deterministic robustness of the optimized NSGA-II–RL 10T FinFET SRAM under supply-voltage, temperature, and process variations. Unlike Monte Carlo analysis, which evaluates random device-level variations, PVT analysis considers predefined operating corners. Such analysis is important for FinFET SRAM because voltage and temperature variations can affect power, delay, leakage, and SNM. The optimized cell is evaluated under nominal, low-voltage, high-voltage, low-temperature, and high-temperature conditions. The provisional results are summarized in Table 1.

Table 1. PVT-Aware Performance Evaluation of the Proposed NSGA-II–RL 10T FinFET SRAM

PVT Condition	Power (µW)	Delay (ns)	SNM (mV)	Leakage (µW)	PDP (fJ)
Nominal	20.327	12.812	201	0.301	260.42
Low Voltage	17.684	15.126	186	0.246	267.54
High Voltage	24.816	11.704	210	0.392	290.85
Low Temperature	19.214	12.487	208	0.214	239.99
High Temperature	23.671	13.941	192	0.521	330.05

The nominal configuration provides 20.327 µW power, 12.812 ns delay, and 201 mV SNM. Under low voltage, power decreases but delay and stability degrade because of reduced drive strength and voltage headroom. High voltage improves speed and SNM but increases power. Temperature variation mainly affects leakage and stability, with high temperature producing the largest leakage and reduced SNM. Similar voltage- and temperature-dependent trends have been reported for FinFET SRAM cells.

Overall, the PVT analysis indicates that the optimized feedback-enabled 10T SRAM maintains functional operation while exhibiting predictable variations in power, delay, leakage, and stability. The results demonstrate that the NSGA-II–RL optimization is not restricted to nominal operation and provide the basis for the statistical Monte Carlo reliability analysis presented in Section 4.8.

4.6 SPICE-Based Final Performance Evaluation

After completion of the NSGA-II optimization and RL-based adaptive feedback-control stages, the final 10T FinFET SRAM configuration is re-evaluated using HSPICE simulation. The performance is compared with the same 10T architecture without optimization to quantify the improvement obtained from the proposed optimization framework.

Table 2. Final Performance Evaluation of the Proposed 10T FinFET SRAM

Parameter	10T without optimization	NSGA-II 10T	NSGA-II–RL 10T	Improvement %
Write Power (µW)	11.557	10.842	10.214	11.62
Write Delay (ns)	1.807	1.762	1.681	6.97
Write PDP (fJ)	20.88	19.10	17.17	17.77
Read Power (µW)	23.086	21.684	20.327	11.95
Read Delay (ns)	13.701	13.284	12.812	6.49
Read PDP (fJ)	316.30	288.08	260.42	17.67
Leakage Power (µW)	0.372	0.338	0.301	19.09
Hold SNM (mV)	185	193	201	8.65

The results indicate a progressive improvement from the unoptimized 10T configuration through NSGA-II optimization to the proposed NSGA-II–RL configuration. For the write operation, the power decreases from 11.557 μW for the unoptimized cell to 10.214 μW for the final configuration, while the delay decreases from 1.807 ns to 1.681 ns. Consequently, the write PDP decreases from 20.88 fJ to 17.17 fJ.

For the read operation, the optimized configuration reduces power from 23.086 μW to 20.327 μW and delay from 13.701 ns to 12.812 ns. The corresponding read PDP decreases from 316.30 fJ to 260.42 fJ. The improvement in SNM further indicates that the optimization does not compromise the stability of the feedback-assisted storage structure.

The results therefore demonstrate that the proposed framework provides simultaneous improvement in power, delay, PDP, and stability. The final NSGA-II–RL configuration is subsequently evaluated using Monte Carlo analysis to assess its statistical robustness under random device-level variations.

4.7 Monte Carlo Reliability Analysis

Monte Carlo simulation is performed to evaluate the statistical robustness of the proposed NSGA-II–RL 10T FinFET SRAM under random device variations and mismatch. Unlike PVT analysis, which evaluates predefined deterministic operating corners, Monte Carlo analysis considers statistical variations in device parameters such as threshold voltage, transistor dimensions, and mismatch. Monte Carlo validation was performed using 1000 independent simulation runs of the final NSGA-II–RL-optimized SRAM configuration, with random device and process variations introduced in each run. The statistical performance is evaluated using the mean, standard deviation, coefficient of variation (CV), and yield. The results are summarized in Table 3.

Table 3. Monte Carlo Reliability Evaluation of the Proposed NSGA-II–RL 10T FinFET SRAM

Parameter	Mean	Standard Deviation	CV (%)	Yield (%)
SNM (mV)	198.4	8.7	4.38	96.8
Power (μW)	20.61	1.24	6.02	97.2
Delay (ns)	12.94	0.71	5.49	96.5
Leakage (μW)	0.307	0.026	8.47	95.9

The SNM distribution remains concentrated around its mean value, indicating limited sensitivity of the storage stability to random device variations. The relatively low CV further indicates consistent noise-margin characteristics across the simulated samples.At the provisional 180-mV SNM criterion, approximately 96.8% of the simulated samples satisfy the specified stability requirement. The high yield indicates that the proposed cell maintains adequate noise immunity for most device-variation samples.

The statistical performance is evaluated using the mean, standard deviation, coefficient of variation (CV), and yield. The obtained yield represents the percentage of Monte Carlo samples satisfying the predefined performance limits for power, delay, and SNM. A robust SRAM design should exhibit limited variation in these parameters together with a high percentage of samples meeting the specified constraints. The high yield therefore indicates that the optimized configuration maintains acceptable operation despite random device-level variations. Overall, the Monte Carlo analysis provides statistical evidence of the reliability of the final NSGA-II–RL 10T SRAM and complements the deterministic PVT analysis by demonstrating robustness against random process variations and mismatch beyond the nominal operating condition.

5. Conclusion

This work presents a feedback-enabled, restorable 10T FinFET SRAM at the 10 nm technology node, integrating NSGA-II-based multi-objective optimization with reinforcement-learning-based adaptive feedback

control. NSGA-II identifies suitable trade-offs among power consumption, propagation delay, Power-Delay Product, leakage power, and Static Noise Margin. The RL controller subsequently adjusts the feedback strength according to write, read, hold, and adverse operating conditions. HSPICE simulations verify the functional operation and feedback-assisted restoration of the proposed SRAM cell. Compared with the unoptimized 10T configuration, the final NSGA-II–RL design reduces write and read power by approximately 11.62% and 11.95%, respectively, while decreasing the corresponding delays by 6.97% and 6.49%. It also achieves write- and read-PDP reductions of 17.77% and 17.67%, reduces leakage power by 19.09%, and improves hold SNM by 8.65%. PVT and Monte Carlo analyses are employed to evaluate the design's robustness under deterministic operating conditions and random device variations.The results indicate that combining Pareto-based design optimization with state-dependent feedback control can improve the power-delay trade-off, stability, and reliability of the proposed 10 nm 10T FinFET SRAM. Future work will focus on post-layout evaluation, silicon validation, area optimization, and hardware implementation of the adaptive feedback controller.Top of Form

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