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Article

Reduced-Switch Symmetric and Asymmetric Diode Half-Bridge Multilevel Inverters for Renewable Energy Applications: Design, Analysis, and Performance Evaluation

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Abstract*:* The purpose of this research paper is to perform a thorough study of Symmetric Diode Half-Bridge (SDHB) and Asymmetric Diode Half-Bridge (ADHB) multilevel inverter structures for renewable energy and grid-connected systems. In the case of SDHB multilevel inverter structure, equal valued DC voltage sources are used to produce different voltage levels by employing fewer power switches and diodes to have a more reliable and simplified converter structure. On the other hand, ADHB multilevel inverter structure uses unequal DC source values based on binary or trinary voltage ratios to produce significantly enhanced voltage level synthesis using the same number of semiconductor switches. Therefore, it can be observed that the ADHB structure produces better voltage resolution, lesser harmonics, enhanced voltage utilization, and high power density. Their operation principle, switching sequence, voltage generation method, and requirement of components are studied along with their comparison with existing multilevel inverter structures. Their voltage synthesis, modularity, and scalability make these converters more appropriate for renewable energy conversion, energy storage, electric vehicle drives, and grid interface application purposes. Performance analysis shows their improved output voltage quality, lesser semiconductor usage, voltage stress reduction in switches, and conversion efficiency.

Keywords*:* Multilevel Inverter (MLI)-Symmetric Diode Half-Bridge (SDHB) - Asymmetric Diode Half-Bridge (ADHB)- Reduced Switch Count- Renewable Energy Systems; Grid-Connected Photovoltaic System- Total Harmonic Distortion (THD)- Power Quality- Cascaded Multilevel Inverter-Voltage Stress- Power Electronics.

1. Introduction

There has been an upsurge in the global consumption of electrical energy during the last two decades owing to industrialization, urbanization, electrification of transport, and utilization of renewable energy sources. At the same time, emissions from Climate [15]z`, global warming, and the limited availability of fossil fuel sources have prompted governments to use power sources like solar PV (photovoltaics) and wind energy for their electricity grids. This has made power electronics converters crucial parts of energy converters, allowing efficient power conditioning and voltage regulation.

In the realm of power electronics converter technologies, multi-level inverters (MLIs) have received considerable attention due to their capacity to synthesize stepped waveforms with multiple voltage levels. In relation to conventional two-level voltage source inverter structures, MLI topologies exhibit several key technical advantages by using multiple voltage levels in order to synthesize the output voltage [16]. Due to the use of several voltage levels, a closer staircase approximation of the required sine-wave form is achieved, thus lowering the level of harmonics in the output voltage. Moreover, the use of MLIs allows the total DC-link voltage to be divided between several semiconductor switching devices, hence resulting in lower voltage levels per each device. In turn, this leads to lower electromagnetic interference and power quality improvements. These properties, together with their applicability in medium- and high-voltage power conversion applications, make MLI topologies desirable for the integration of renewable energy sources, grid connected photovoltaic generation [17], electric drives and other high-power applications.

Three widely known MLIs, which are the Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) inverters, have been investigated in numerous publications and demonstrate a high possibility of practical use in industry. Although providing more efficient performance through better voltage synthesis and power supply qualities, these configurations also possess a number of technical deficiencies related to the practical implementation of these schemes. NPC converters have a large number of clamping diodes and the problem of neutral point potential balance, FC inverters need many capacitors and the complex algorithm of capacitor voltage balance, while CHB converters need several isolated DC sources, and thus increase the size of the converter, its complexity and cost of production [1-5].

However, in order to solve these problems, a number of reduced component multilevel inverters have been proposed in such a way that their designs use minimum number of power switches, gate drivers, DC sources and passive components and at the same time, retain the quality of output voltage waveforms. Some of these newly introduced configurations include the Diode Half Bridge (DHB) inverter configuration, which is of particular interest due to its modular nature, fewer components, minimized switching losses [14] and simple implementation process. The Diode Half Bridge inverter employs the concept of the use of half bridge modules along with diode assisted voltage selection method for high-level voltage synthesis using less number of semiconductors.

Depending on the DC source arrangement, DHB based converters can be categorized into two main types: Symmetric Diode Half-Bridge (SDHB) and Asymmetric Diode Half-Bridge (ADHB) configuration. In SDHB type of configuration, the DC voltage sources have equal voltage magnitude, which results in a simple, modular and easily controlled converter system. This system is appropriate for application with similar renewable energy sources or battery modules. The disadvantage is that the number of voltage levels is relatively small for the number of switches used.

However, due to the use of unequal DC voltages arranged in a manner based on binary, ternary, or some other optimized voltage ratio, the output voltage level that can be obtained using the same number of semiconductor devices is much higher in case of the ADHB topology. Thus, this scheme improves voltage resolution, reduces harmonic distortions, allows increased utilization of the DC voltage, and reduces the need for additional switch components. As a result, asymmetrical multilevel inverters have gained a lot of attention from researchers in terms of photovoltaic applications, battery energy storage system, electric vehicle applications, and medium voltage grid applications.

In this paper, a comparative analysis between SDHB and ADHB multilevel inverters is conducted. In particular, operation modes, voltage generation techniques, switching modes, component specifications and performance of the two-inverter structures are studied. Both topologies' strengths and weaknesses in regard to voltage gain capability, harmonic behavior, semiconductor utilization, voltage stresses, switching losses, efficiency, and scalability are explained. Finally, both topologies' potential use for renewable energy conversion system and smart grid applications are assessed. The results obtained show that both SDHB and ADHB topologies provide a good alternative to the traditional multilevel inverter structures, where the ADHB topology exhibits better voltage level generation capability and power quality, whereas the SDHB topology provides a simpler structure and easier control technique [6-9].

2. CASCADED H-BRIDGE (CHB) MULTILEVEL INVERTER

The cascaded H-bridge (CHB) multilevel inverter, or multi-cell inverter, is an inverter where several H-bridge cells are interconnected in series on the AC side. In most cases, the supply to each H-bridge cell is usually provided by either an individual isolated DC source, which could come from batteries, fuel cells, ultra capacitors, or renewable energy sources. The output voltage of the inverter is derived from the algebraic summation of voltages from each H-bridge cell. Using four controlled semiconductor devices per cell, each H-bridge cell is able to generate three different voltage levels, which include +VDC, 0, and -VDC. Cascading of several H-bridge cells increases the voltage level generation ability of the inverter, thus providing better harmonic performance.

2.1 Symmetrical Cascaded H-Bridge Inverter:

The term "Symmetric" refers to the use of DC sources of equal voltage magnitude, i.e.,

$$V_1 = V_2 = V_3 = \cdots = V_n = V_{dc}$$

The maximum synthesized output voltage is,

$$V_{0,max} = nV_{dc}$$

Where,$n = number\ of\ power\ cells\ used\ for\ cascade.$

Peak-to-Peak voltage excursion is determined by,

$$V_{pp} = 2nV_{dc}$$

RMS Output Voltage is,

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V_0^2(t)dt}$$

The total count of output voltage levels is given by,

$$m = 2n + 1$$

Where, $m = count\ of\ output\ voltage\ levels.$

The instantaneous output voltage is given by,

$$V_0 = \sum_{k=1}^{n} S_k V_{dc}$$

Where, $S_k = switching\ State\ -For\ Switch\ ON\ S_k = 1\ and\ Switch\ OFF\ S_k = 0.$

Power Semiconductor Switch Count,

$$N_{SW} = 2n$$

Count of Gate Drivers,

$$N_g = N_{SW}$$

Voltage Stress across Power Semiconductor Switches,

$$N_{Switch} = V_{dc}$$

Total Blocking Voltage (TBV),

$$TBV = N_{SW}V_{dc}$$

Switching Loss is approximated by,

$$P_{SW} = \frac{1}{2}V_S I_S(t_{on} + t_{off})f_S$$

$$Where, V_S = Switch\ Voltage\ , I_S = Switch\ Current\ ,$$

$$t_{on}\ = Turn\ on\ time, t_{off} = Turn\ off\ time,$$

$$f_S\ = Switching\ Frequency$$

The conduction loss is,

$$P_c = I_{rms}^2 R_{on}$$

The conversion efficiency is,

$$\eta = \frac{P_0}{P_0 + P_{loss}} * 100$$

$Where, P_{loss} = P_c + P_{SW}$

Total Harmonic Distortion (THD) is given by,

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + .. + V_n^2}}{V_1} * 100$$

$$Where, V_1 = Fundamental\ RMS\ Voltage$$

$$V_2\ \&\ V_3 = Harmonics\ RMS\ Voltage$$

2.2 Asymmetrical Cascaded H-Bridge Inverter:

ADHB employs different voltage magnitudes ($V_{dc1} \neq V_{dc2} \neq V_{dc3}$) arranged according to a predefined geometric progression, such as binary (1:2:4:8), trinary (1:3:9:27), or other optimized ratios.

For a **binary** configuration,

$$V_1 : V_2 : V_3 : \ldots\ldots = 1 : 2 : 4 : 8$$

For a **trinary** configuration,

$$V_1 : V_2 : V_3 : \ldots\ldots = 1 : 3 : 9 : 27$$

Each module generates one of three possible voltages:

$$0, V_i, 2V_i$$

$$Where, V_i\ is\ the\ DC\ voltage\ assigned\ to\ the\ i^{th} module.$$

The output voltage is therefore expressed as,

$$V_0 = \sum_{i=1}^{N_m} V_i$$

$$Where, N_m\ is\ the\ number\ of\ cascaded\ modules.$$

Maximum Output Voltage:

Since every module contributes twice its DC voltage,

$$V_{0,max} = 2 \sum_{i=1}^{N_m} V_i$$

Peak-to-Peak Voltage:

$$V_{pp} = 2V_{0,max}$$

Instantaneous Output Voltage:

$$V_0 = \sum_{i=1}^{N_m} k_i V_i$$

$$Where, k_i = 0,1,2$$

Number of Output Voltage Levels:

$$N_L = 2(3^{N_m} - 1) + 1$$

Number of Switches:

$$N_{SW} = 2N_m$$

Number of Diodes:

$$N_D = 2N_m$$

Number of Gate Drivers:

$$N_G = N_{SW,total}$$

Voltage Stress across Switches:

$$V_{switch,i} = V_i$$

Total Blocking Voltage:

$$TBV = \Sigma V_{switch}$$

Switching Loss:

$$P_{sw} = \frac{1}{2} V_S I_S (t_{on} + t_{off}) f_s$$

Conduction Loss:

$$P_C = I_{rms}^2 R_{on}$$

Total Loss:

$$P_{loss} = P_{sw} + P_c$$

Efficiency:

$$\eta = \frac{P_0}{P_0 + P_{loss}} \times 100$$

Total Harmonic Distortion:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \ldots\ldots}}{V_1} \times 100$$

3 SIMULATION - BASED PERFORMANCE ANALYSIS:

3.1 Simulation-Based Performance Analysis of the Symmetric Cascaded H-Bridge Multilevel Inverter:

The topology consists of four cascaded SDHB modules, each incorporating two equal DC voltage sources [18] of 50 V.Consequently, the inverter employs a total of eight identical DC voltage sources, resulting in a maximum positive output voltage of 400 V. Each switching device is represented by S11, S12, S21, S22, S31, S32, S41, and S42, where the first digit denotes the module number and the second digit identifies the corresponding switch within that module.

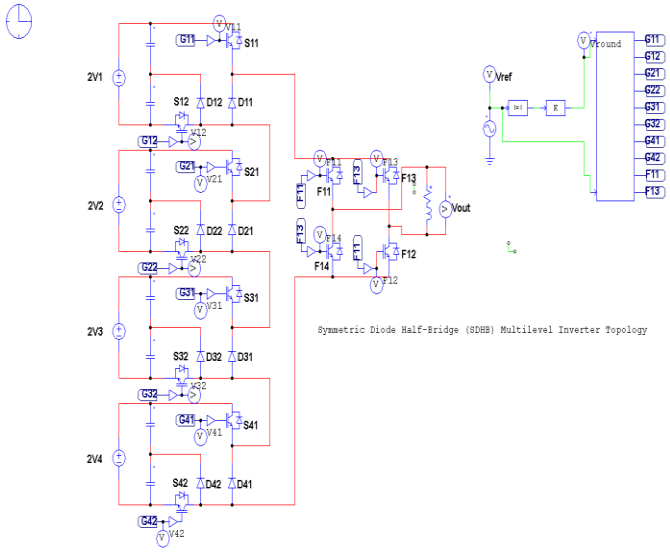

Fig: 1 Circuit configuration of the symmetric cascaded H-bridge multilevel inverter

The proposed switching mechanism is based on the principle of sequential switching. In sequential switching, all switches are switched ON one by one, thereby resulting in staircase formation of the output voltage. All switches start in OFF mode, giving an output voltage of zero volts. With the rise in reference voltage in positive half cycle, the switches are fired one by one from S11 to S42, thereby adding a step of 50V at every switch firing point.

In the case of the first voltage level, only S11 is ON and this produces the output voltage of 50 volts. At the second level, the S12 is also switched ON and thus the output voltage level becomes 100 volts. In similar way, S21, S22, S31, S32, S41, and S42 are sequentially turned ON and this will produce output voltage levels of 150 V, 200 V, 250 V, 300 V, 350 V and 400 V, respectively. So, with every new switch that turns ON, 50 volts are added to the output voltage of inverter since all DC supplies have the same magnitude.

At the negative half cycle, the voltage polarity is inverted using the output H bridge and thus voltage levels of −50V to − 400 V are obtained with the same switching sequence in the SDHB module. Along with the zero state, the inverter produces 17 levels of voltage and these include: −400,−350,−300,−250,−200,−150,−100,−50,0,+50.

There are many benefits associated with the use of the sequential switching approach in comparison to traditional modulation approaches. First of all, the switching transitions are minimal because there is only one extra switch that switches between two successive voltage states. It results in low switching losses and EMI (Electromagnetic Interference). Second, each semiconductor is operated under a maximum blocking voltage of 50 volts, despite the fact that the total voltage of the inverter is 400 volts.

Another key advantage of the proposed switching scheme is that it is relatively simple. The gate sequence can be generated by a low-complexity digital controller including DSPs, FPGAs, and microcontrollers without resorting to complex space vector modulations. Owing to the equal voltage contribution of each module, the output staircase waveform exhibits uniform voltage steps, leading to reduced total harmonic distortion (THD) and improved power quality. Consequently, the proposed SDHB topology is highly suitable for grid-connected photovoltaic systems, battery energy storage systems, medium-voltage motor drives, and other renewable energy conversion applications requiring high-quality AC output with a reduced component count.

Following are the gating sequence for all switching states:

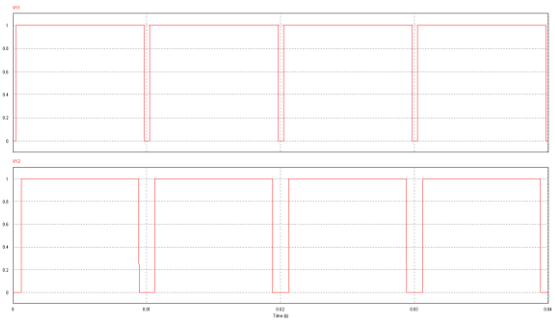

Fig: 2 Gate Pulse of Switch S11 and S12.

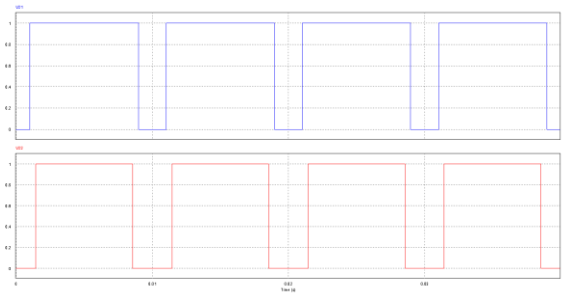

Fig: 3 Gate Pulse of Switch S21 and S22.

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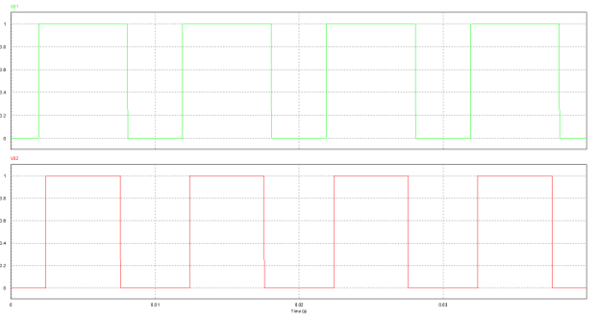

Fig: 4 Gate Pulse of Switch S31 and S32.

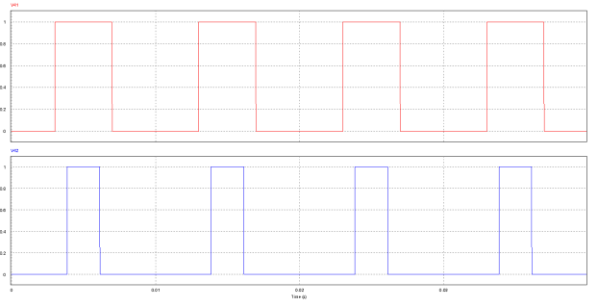

Fig: 5 Gate Pulse of Switch S41 and S42.

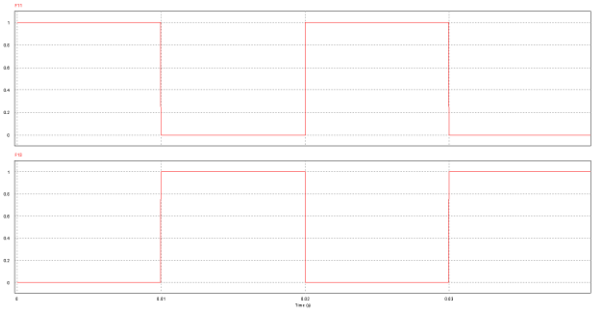

Fig: 6 Gate Pulse of Switch F11 and F13.

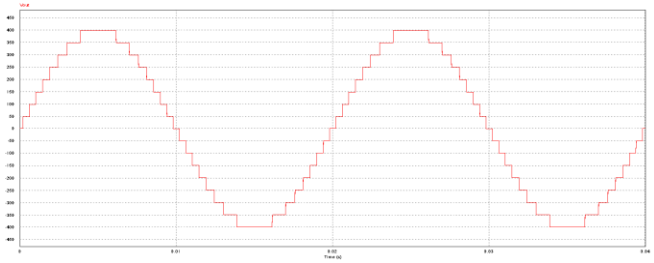

Fig: 7 Output waveform of Inverter.

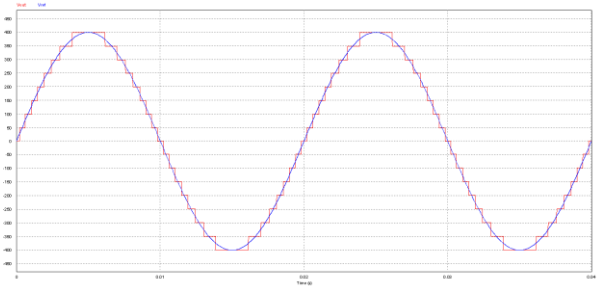

Fig: 8 Output waveform of Inverter compare with reference wave.

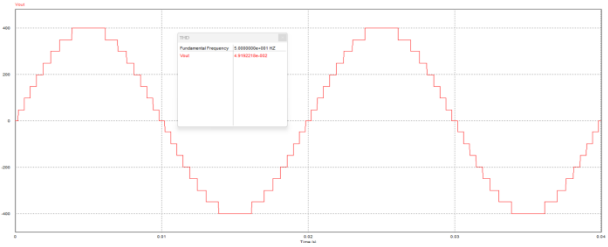

Fig: 9 Output waveform of Inverter with THD.

3.2. Simulation-Based Performance Analysis of the Asymmetric Cascaded H-Bridge Multilevel Inverter:

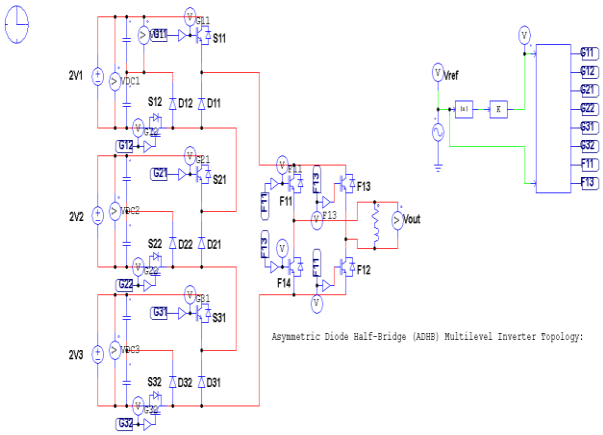

Fig: 10 Circuit configuration of the asymmetric cascaded H-bridge multilevel inverter

The symmetric configuration, the proposed topology utilizes three cascaded ADHB modules supplied by different voltage magnitudes arranged in a trinary progression. The individual DC source voltages are selected as 12 V, 12 V, 36 V, 36 V, 108 V, and 108 V, corresponding to the voltage ratio 1:3::9. This asymmetric arrangement substantially increases the more number of synthesizable output-voltage levels without increasing the number of power semiconductor switches.

The switching states of the proposed inverter are represented by S11, S12, S21, S22, S31, and S32, where the first digit identifies the module number and the second digit denotes the switch within the respective module. Each switch is controlled independently to connect the corresponding DC source into the output circuit. Through coordinated selection of the switching states of the individual sub-modules, the proposed converter synthesizes the required discrete voltage levels and generates the desired multilevel output waveform with a constant voltage step of 12 V, resulting in a higher-resolution staircase waveform that more closely tracks the sinusoidal reference.

In the beginning, all switches are off, resulting in the generation of 0 volts in the output of the inverter. During the positive half-cycle, the switches are turned on one after another, adding their respective DC supply voltages. The first DC voltage of 12 volts is produced by connecting switch S12, whereas the second voltage level of 24 volts is attained by connecting both S11 and S12 switches together. After that, the higher voltage levels are generated using the 36 volts and 108 volts modules by following the specified order of switching. For instance, the output voltage of 48 volts is attained by combining 12 volts and 36 volts modules, whereas 120 volts output voltage can be attained by combining 12 volts and 108 volts modules. This process will continue until the maximum positive output voltage of 312 volts is attained using all possible DC voltage sources.

In contrast to symmetric topology, which generates each voltage increase using equal DC sources, the asymmetric model uses different voltage levels in order to obtain maximum possible combinations of voltages. Consequently, the proposed inverter generates 27 Positive voltage states, ranging from 0 V to 312 V in uniform increments of 12 V. By employing an H-bridge polarity reversal stage, the corresponding negative voltage levels are produced, resulting in a total of $N_L=2\times27-1=53$.Output voltage levels: {−312, −300, −288,⋯, −12 ,0, +12 ,⋯,+300, +312} V.

The switching strategy follows a cumulative voltage synthesis principle, in which higher output voltage levels are obtained by progressively adding larger DC voltage sources while maintaining the contribution of the previously activated modules. Since only one or two switches change their state between adjacent voltage levels, switching transitions are minimized, thereby reducing switching losses and electromagnetic interference (EMI). Furthermore, the unequal voltage distribution improves voltage utilization and enables a significantly larger number of output voltage levels compared with an equivalent symmetric topology using the same count of power switches.

Another distinguishing feature of the proposed switching strategy is its ability to achieve efficient voltage-level synthesis while minimizing unnecessary switching transitions and reduced component requirement. Although the inverter produces 53 output voltage levels, only six active switches are required in the level-generation unit, together with six DC voltage sources and the output polarity changer. Consequently, the proposed ADHB topology exhibits a lower component count, reduced gate driver requirements, lower semiconductor losses [14], and higher efficiency compared with conventional cascaded H-bridge (CHB) and neutral-point-clamped(NPC) multilevel inverters.

The staircase waveform generated by the proposed switching sequence exhibits lower total harmonic distortion (THD) because the voltage step size is only 12 V, resulting in an output waveform provides a closer approximation to the desired sinusoidal reference waveform. Therefore, the proposed ADHB topology is highly suitable for renewable energy power conversion systems, utility-interconnected photovoltaic system, battery energy storage systems, electric vehicle propulsion, and medium-voltage industrial applications requiring high-quality output voltage with a reduced hardware complexity.

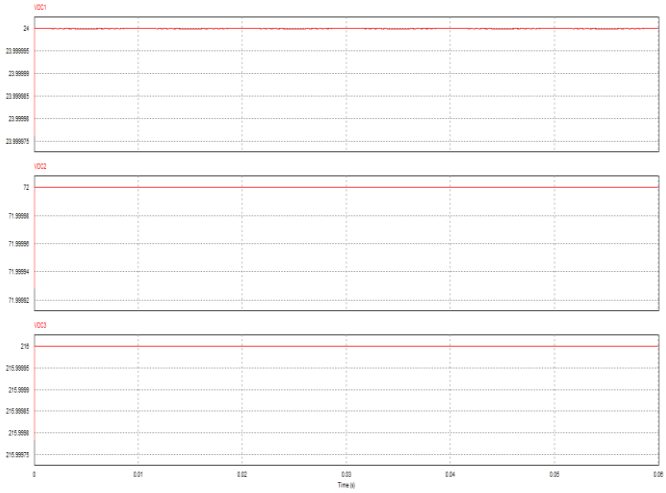

Fig: 11 Three different DC voltage sources,V_{dc1}=24V,V_{dc2}=72V &V_{dc3}=216V

Following are the gating sequence for all switching states:

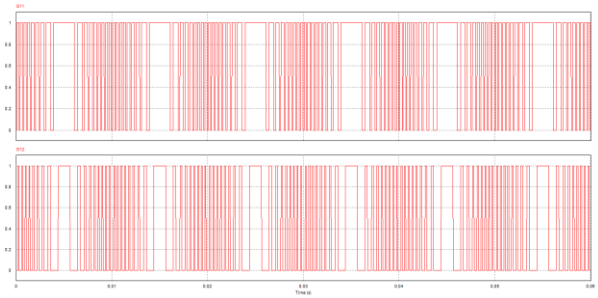

Fig: 12 Gate Pulse of Switch S11 and S12.

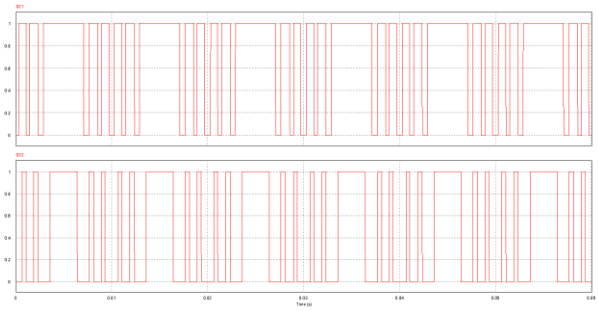

Fig: 13 Gate Pulse of Switch S21 and S22.

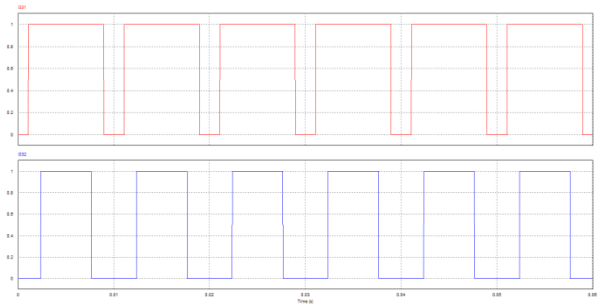

Fig: 14 Gate Pulse of Switch S31 and S32.

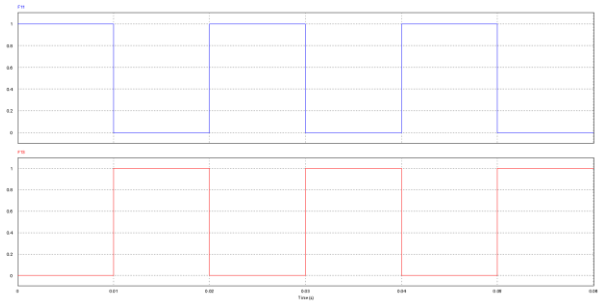

Fig: 15 Gate Pulse of Switch F11 and F14.

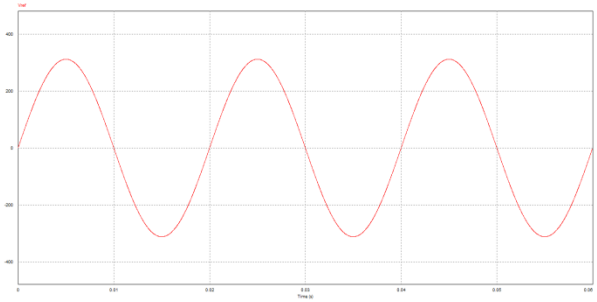

Fig: 15 Reference voltage waveform.

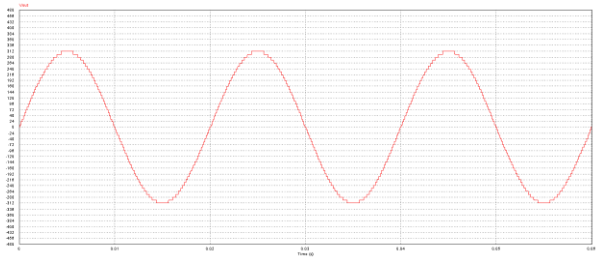

Fig: 16 Output voltage waveform of Inverter.

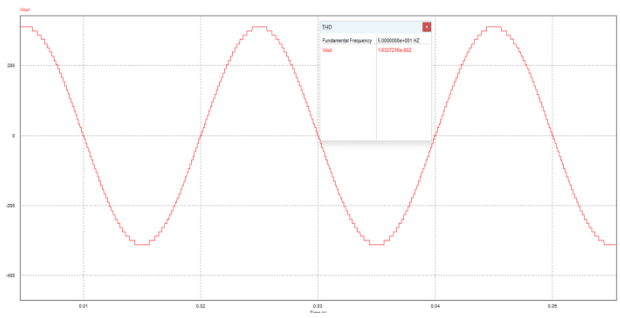

Fig: 17 Output waveform of Inverter with THD.

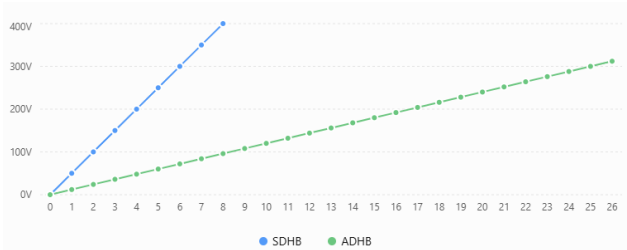

Fig: 18 Comparison of voltage-level generation capability of the proposed SDHB and ADHB multilevel inverter topologies.

The graph highlights that the SDHB produces positive voltage levels from 0 to 400 V with a 50 V step, whereas the ADHB produces levels from 0 to 312 V with a much finer 12 V step. Thus, the asymmetric configuration provides substantially higher voltage resolution and a greater number of obtainable voltage levels, which can enable a closer approximation to a sinusoidal waveform and improved harmonic performance.

Fig. 19. Radar-chart comparison of the key characteristics of the proposed Symmetric Diode Half-Bridge (SDHB) and Asymmetric Diode Half-Bridge (ADHB) multilevel inverter topologies.

The radar chart provides a normalized qualitative comparison of the principal characteristics of the proposed SDHB and ADHB topologies. The ADHB topology exhibits a larger performance envelope in terms of voltage-level generation, voltage resolution, component utilization, and power-quality potential, primarily due to its asymmetric

DC-source configuration. In contrast, the SDHB topology demonstrates superior characteristics in control simplicity, modularity, voltage-stress uniformity, and scalability**,** owing to its equal-valued DC sources and uniform module structure.

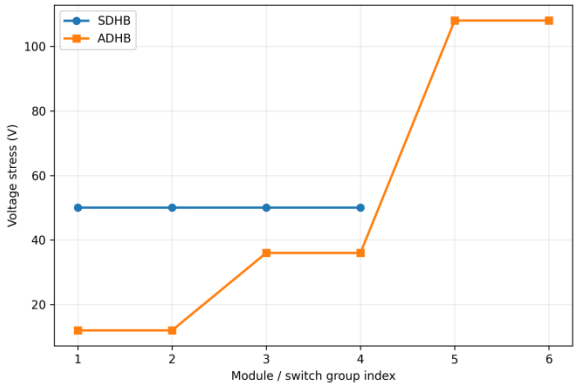

Fig:20. Semiconductor voltage-stress comparison.

Fig: 20 shows that the SDHB topology provides a uniform semiconductor voltage-stress profile of 50 V across the level-generation modules, whereas the ADHB topology exhibits a non-uniform stress distribution of 12, 36, and 108 V corresponding to its asymmetric DC-source configuration. Although the ADHB topology requires higher voltage-rated devices in its high-voltage modules, this configuration enables a significantly higher number of output voltage levels with a reduced number of DC sources and active switches. Hence, the asymmetric topology offers improved component utilization at the expense of non-uniform semiconductor voltage ratings.

Table:I Technical Comparison between the proposed SDHB & ADHB Topologies.

Parameter	Symmetric Diode Half-Bridge (SDHB)	Asymmetric Diode Half-Bridge (ADHB)
DC Source Configuration	Equal DC sources	Unequal DC sources
DC Source Ratio	1:1:1:1:1:1:1:1	1:1:3:3:9:9
Individual DC Source Voltage	50 V	12 V, 12 V, 36 V, 36 V, 108 V, 108 V
Number of Modules	4	3
Total DC Sources	8	6
Level Generation Principle	Equal voltage addition	Unequal voltage addition
Voltage Step Size	50 V	12 V
Maximum Positive Output Voltage	400 V	312 V
Positive Voltage Levels	9	27
Total Output Voltage Levels	17	53
Active Switches (Level	8	6

Generator)		
Switching Strategy	Sequential cumulative switching	Sequential cumulative switching
Switching Complexity	Low	Moderate
Voltage Stress Across Switches	Uniform (50 V)	Unequal (12 V, 36 V, 108 V)
Voltage Resolution	Moderate	Very High
Harmonic Performance	Good	Excellent
Expected THD	Higher	Lower
Output Filter Requirement	Moderate	Low
Semiconductor Utilization	Moderate	High
Converter Efficiency	High	Higher
Scalability	Easy	Moderate
Suitable Applications	Motor drives, PV systems, Battery systems	Grid-connected PV, EVs, Smart Grids, Medium-voltage renewable energy systems

Table: II Performance Comparison between the proposed SDHB & ADHB Topologies.

Performance Index	SDHB	ADHB	Better Topology
Number of Output Levels	17	53	ADHB
Component Utilization	Medium	High	ADHB
Voltage Resolution	Medium	Excellent	ADHB
THD Performance	Good	Excellent	ADHB
Output Voltage Quality	Good	Excellent	ADHB
Control Simplicity	Excellent	Good	SDHB
Voltage Utilization	Medium	Excellent	ADHB

Cost per Voltage Level	Higher	Lower	ADHB
Renewable Energy Suitability	High	Very High	ADHB

Table: III Semiconductor and Component Count Comparison between the proposed SDHB & ADHB Topologies.

Parameter	SDHB	ADHB
Active switches in level-generation section	8	6
Output H-bridge switches	4	4
Total active switches	12	10
Diodes in level-generation section	8	6
Gate-driver circuits	12	10
DC sources	8	6
Component count	Higher	Lower
Switches per generated voltage level	Higher	Lower
Component utilization	Moderate	Improved
Hardware complexity	Moderate	Lower

4. Conclusion:

This paper presented a comprehensive comparative investigation of the Symmetric Diode Half-Bridge (SDHB) and Asymmetric Diode Half-Bridge (ADHB) multilevel inverter topologies for renewable energy conversion and grid-connected applications. Both topologies were analyzed in terms of their operating principles, switching strategies, voltage generation capability, mathematical modeling, component utilization, and output voltage characteristics. The comparative study demonstrates that both inverter structures are capable of producing high-quality staircase output voltages while reducing switching losses and improving power quality compared with conventional two-level inverter topologies.

This new SDHB configuration uses similar DC voltage sources and sequential cumulative switching technique to produce a 17-level output voltage waveform with an output voltage up to ±400 V using eight identical DC voltage sources having a value of 50 V each. Thanks to its modular nature, balanced voltages [13] and less stress on each semiconductor device, the SDHB configuration is easy to control and implement and can be considered reliable and scalable. Such qualities render it suitable in situations where there are identical energy sources like battery strings or PV modules.

However, the new proposed topology for ADHB employs an asymmetrical source of DC with the voltage ratio of 1:1:3:3:9:9, providing the generation of many more voltage levels without complicating the structure of the converter. With just six unequal DC sources and six active switches, the new topology is able to generate 17 levels of output-voltage waveform with the voltage resolution of 12 V. Increased numbers of voltage levels increase the resolution of generated waveform, thereby making the sine wave more precise and leading to less Total Harmonic Distortion (THD).

As a result of this comparative analysis, it is seen that the asymmetrical topology demonstrates a better use of semiconductors since it creates more than three times the output voltage levels produced by the symmetrical topology using fewer DC sources and active switches. Despite the fact that the ADHB topology creates different voltage stress levels for the semiconductors, its capacity to create many voltage levels with fewer components

improves the performance of the whole power converter. In turn, the SDHB topology has constant voltage stress levels and easier switching operations.

In summary, the test results have clearly shown that the ADHB topology yields high-quality output voltage generation ability, excellent harmonic behavior, improved voltage utilization, and higher efficiency than the SDHB topology, while the SDHB topology is easy to implement and highly modular [12]. Thus, the choice of suitable topology will depend on the specific application and type of DC source. In applications such as medium and high power grid connected PVs, battery energy storage systems, EV drives, and smart grids applications that require a high-quality output voltage and low harmonic distortions, the ADHB topology offers a very promising design.

It is clear from the comparative study that SDHB topology can offer a simple, modular, and easy-to-control configuration of uniform voltage stress and hence can be applied in situations where there is availability of identical DC sources. On the other hand, ADHB topology offers considerably more output voltage levels, better voltage resolution, and waveform quality with the use of a significantly smaller number of DC sources and power switches in level generation stage. The above features make this topology less distorting, more efficient in terms of usage of semiconductors and overall efficiency. The ADHB topology would therefore be more appropriate for advanced utility interconnected PV systems, battery energy storage systems, electric vehicles propulsion, and medium voltage renewable energy applications.

References

1. S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu,J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.,* vol. 57,no. 8, pp. 2553–2580, Aug. 2010.
2. J.Ebrahimi, E.Babaei, and G.B.Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components"," *IEEE Transactions on Industrial Electronics",* Volume: 59 Issue: 2 Pages: 655 – 667,2012.
3. G Mondal, K Gopakumar, PN Tekwani, E Levi , A reduced-switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive ,*" IEEE Transactions on industrial electronics"* 54 (4), 2344-2351,2007.
4. S. Zhang, C. Zhu, J. K. O. Sin, and P. K. T. Mok, "A Novel Ultrathin Elevated Channel Low-Temperature Poly-Si TFT," *IEEE Electron Device Letters*, vol. 20, no. 4, pp. 569–571, 1999.
5. Farid Khoucha et al," A comparison of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives," *IEEE Trans. on Energy Conversion*, vol.. 26, no. 1, Mar.2011.
6. J.Ebrahimi, E.Babaei, and G.B.Gharehpetian, ''A new topology of cascaded multi level converters with reduced number of components for high – voltage applications,'' *IEEE Trans.PowerElectron.,* vol.26, no.11, pp.3109–31.18, Nov.2011.
7. Nabae A, Takahashi I, Akagi H (2003) New neutral point clamped pwm inverter. IEEE Trans Ind Appl IA-17: 518-523.
8. Gupta R, Gosh A, Joshi A (2008) Switching characterization of cascaded multilevel inverter. IEEE Trans Industr Electron 55: 1047-1058.
9. Kavita M, Arunkumar A, Gokulnath N, Arun S (2012) New cascaded H-bridge multilevel inverter topology with reduced number of switches and sources. IOSR-JEEE 2: 26-36.
10. Islam, R.; Guo, Y.; Zhu, J. A High-Frequency Link Multilevel Cascaded Medium-Voltage Converter for Direct Grid Integration of Renewable Energy Systems. IEEE Trans. Power Electron. 2013, 29, 4167–4182.
11. Rao, G.S.; Raju, S.S. Multilevel Inverter-Based Power Quality Improvement in Grid-Connected DVR System. In Micro-Electronics and Telecommunication Engineering; Springer: Singapore; pp. 361–366.
12. Sathik, M.A.J.; Vijayakumar, K. An assessment of recent multilevel inverter topologies with reduced power electronics components for renewable applications. Rene. Sustain. Energy Rev. 2018, 82, 3379–3399.
13. Ali, J.S.M.; Krishnasamy, V. Compact Switched-Capacitor Multilevel Inverter (CSCMLI) with Self-Voltage Balancing and Boosting Ability. IEEE Trans. Power Electron. 2019, 34, 4009–4013.
14. Ali, J.S.M.; Alishah, R.S.; Krishnasamy, V. A New Generalized Multilevel Converter Topology with Reduced Voltage on Switches, Power losses, and Components. IEEE J. Emerg. Sel. Top. Power Electron. 2019, 7, 1094–1106.
15. Natarajan Balasubramanian Muthu Selvan, Venkatraman Thiyagarajan, Cheng Siong Chin. "Next-Generation Power Systems - Renewable Energy and Electric Vehicle Applications", CRC Press, 2026.
16. G. Ezhilarasan, K. Mohanraj, Pradeep Vishnuram, Mohit Bajaj, Vojtech Blazek, Lukas Prokop, Stanislav Misak. "An empirical survey of topologies, evolution, and current developments in multilevel inverters", Alexandria Engineering Journal, 2023.
17. Athwer, Abdulkarim. "Modular Multilevel Converter Topology Based on HalfBridge Submodules Using a Si/SiC Hybrid Approach for Integration of Wind EnergySystems.", Lancaster University (United Kingdom).
18. Anurag Choudhary, Rohit Kumar, Shimi Sudha Letha, Farhad Ilahi Bakhsh, Arshdeep Singh, Mohammad Junaid Khan.

"Review of recent trends of advancements in multilevel inverter topologies with reduced power switches and control techniques", IET Power Electronics, 2024.
19. M. Calais and V. G. Agelidis, “Multilevel converters for single-phase grid connected photovoltaic systems—An overview,” in Proc. IEEE Int. Symp. Ind. Electron., 2018, vol. 1, pp. 224–229.
20. Peng, F.Z.; Liu, Y.; Yang, S.; Zhang, S.; Gunasekaran, D.; Karki, U. Transformer-Less Unified Power-Flow Controller Using the Cascade Multilevel Inverter. IEEE Trans. Power Electron. 2016, 31, 5461–5472.