

A COMPREHENSIVE REVIEW OF CMOS LOW-NOISE AMPLIFIERS FOR SUB-6 GHz WIRELESS RECEIVERS

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Abstract: The low-noise amplifier (LNA), as the first Component of wireless receiver after an antenna, plays a crucial role in deciding the receiver sensitivity, noise figure (NF), gain, linearity, and dynamic range. The evolution of sub-6 GHz wireless systems toward 5G New Radio (NR), Wi-Fi, SAW-less front ends, and IoT has imposed strict and often conflicting requirements for LNA design. This paper reviews major CMOS LNA architectures and their performance trade-offs, with highlighting on linearity enhancement techniques. Previously reported linearization methods were systematically classified into five major categories (a) feedback, (b) feedforward, (c) derivative superposition (DS) including CDS, (d) noise/distortion cancellation, and (e) post distortion. Their effectiveness in suppressing 2nd & 3rd order nonlinearities and improving linearity (IIP2/IIP3) is comparatively discussed. Attention is given to nonlinear transconductance () and output conductance () and deep-submicron CMOS limitations. Recent sub-6 GHz implementations are reviewed to evaluate trade-offs among gain, NF, linearity, bandwidth, power, and area. Finally, key research challenges and future directions toward highly linear, low-noise, wideband, and power-efficient CMOS LNAs are identified.

Keywords: CMOS LNA, sub-6 GHz, 5G NR, linearity

1. Introduction

The RF front end (RFFE) must recover weak desired signals in the presence of thermal noise, adjacent-channel interference, strong blockers, and transmitter leakage. As the first active stage after the antenna, the low-noise amplifier (LNA) dominates the receiver's overall noise performance: for a cascaded chain, the total noise factor follows the Friis relation

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots \quad (1)$$

Where, F = Noise factor of respective stage, G = Power Gain of each respective stage. Eq. (1) explains why the first stage must combine low NF with sufficient gain, since a high-gain LNA suppresses the noise contribution of subsequent stages. Optimizing for minimum NF alone is nonetheless insufficient: strong interferers generate 2nd and 3rd order intermodulation products, gain compression, and desensitization, effects that become more pronounced in short-channel CMOS [2].

Sub-6 GHz CMOS LNA design therefore involves the simultaneous optimization of several contradictory requirements low NF, adequate gain, high linearity, wide or reconfigurable bandwidth, low power, and compact area which grows more difficult in scaled nodes owing to reduced supply voltage, limited voltage headroom, device



parasitic, and PVT sensitivity [2], [3]. To ease these trade-offs, techniques such as broadband noise cancellation [4], [5], [6], g_m boosting [6], current reuse [7], body-floating and self-biasing [8], and post-distortion [9] have emerged as important approaches.

Linearity is particularly critical in recent wideband, multi-standard receivers [3], [10], [11]. Although IIP3 is widely used to characterize nonlinearity, it does not fully describe receiver linearity: 2nd order distortion (IIP2) can become significant in direct-conversion and broadband architectures, the 1-dB compression point (P1dB) captures large signal handling, and in wideband systems linearity varies with both centre frequency (f_c) & interferer tone spacing [4], [12]. A comprehensive comparison must therefore weigh IIP2, IIP3, NF, gain, bandwidth, and power together rather than treating any single metric as sufficient [1], [4], [5].

Accordingly, this review adopts a technique-centric view of sub-6 GHz CMOS LNAs. Conventional topologies are first introduced to establish their operating principles and trade-offs, followed by noise-reduction, gain enhancement, extension of BW, and power-efficiency techniques, and then a systematic treatment of linearization – feedback [13], [14], feedforward [12], derivative superposition [15], noise/distortion cancellation [15], [16], and post distortion [9], with attention to the interaction between noise, gain, linearity, bandwidth, power, and technology scaling [10], [17]. Finally, these techniques are related to contemporary 5G/5G-NR and Wi-Fi requirements and to representative CMOS and SOI implementations [6], [9], [18], [19]. On this basis, key research gaps are identified chiefly the simultaneous achievement of low NF and high linearity under low-voltage, low-power constraints along with the need for consistent measurement and reporting practices when benchmarking published designs [3]. The review paper is organized as follows. Section 2 reviews the fundamentals and performance metrics of the LNA. Section 3 surveys CMOS LNA architecture, and Section 4 examines techniques to reduce noise, gain, and power. Section 5 analyzes linearity and distortion in CMOS LNAs and detailed review of linearity-improvement techniques. Section 6 discusses recent sub-6 GHz LNA developments. Section 7 identifies research gaps and future research directions, and Section 8 concludes the paper.

2. Fundamentals and Performance Metrics

The performance of a CMOS LNA is set by a few tightly coupled metrics – noise, gain, input matching, linearity, and power consumption [1] where improving one typically reprimands another. A meaningful assessment of a sub-6 GHz CMOS LNA therefore depends on weighing these trade-offs jointly rather than on any single headline number [3], [10]. The following subsections review each fundamental parameter in this light.

2.1 Noise Figure (NF): The noise factor is a fundamental parameter for evaluating the noise performance of an LNA and is defined [1] [3],

$$F = \frac{SNR_{in}}{SNR_{out}} \quad (2)$$

The noise figure (NF), expressed in decibels, is given by,

$$NF = 10 \log_{10}(F) \quad (3)$$

For a two-port, the noise behavior is fully described by four noise parameters through [5],

$$F = F_{min} + \frac{R_n}{G_S} |Y_S - Y_{opt}|^2 \quad (4)$$

where F_{min} is the minimum noise factor, R_n the equivalent noise resistance, Y_{opt} the optimum source admittance, and G_S the real part of the source admittance Y_S . Since the noise optimum source impedance ($|Y_S = Y_{opt}|$) generally differs from the impedance for maximum power transfer or best S_{11} , In narrowband common-source LNAs, inductive source degeneration is widely used because it synthesizes a real input term without adding noise, enabling a simultaneous noise and input match [1].

2.2 CMOS Noise Sources: The overall noise performance is set by several device- and circuit-level mechanisms [1], [2],

- **Channel thermal noise:** The drain-current thermal noise of a MOS transistor is commonly represented by [1],

$$i_d^2 = 4kT\gamma g_{d0}\Delta f, \quad (5)$$

where k = Boltzmann's constant, T = absolute temperature, γ = channel thermal noise coefficient, g_{d0} = zero bias drain conductance, and Δf = noise bandwidth.

- **Induced gate noise:** At RF frequencies, the time-varying channel charge produces induced gate noise. This noise is correlated with channel thermal noise and must therefore be considered in accurate RF noise modelling and optimization. [1], [2].
- **Gate and interconnect resistance noise:** The finite resistance of the gate, polysilicon structures, metal interconnects, and other lossy RF components introduces additional thermal-noise contributions. These effects can become increasingly important in high-frequency and compact CMOS implementations [1].
- **Flicker noise:** noise is particularly important in direct-conversion and low-IF receiver architectures because low-frequency noise components can be translated into or appear near the desired baseband signal. Its impact depends strongly on the transistor technology, bias conditions, device dimensions, and receiver architecture. [2].

2.3 Gain and Input Matching: Gain and input matching are two fundamental requirements of an RF LNA. For a CS amplifier, a first-order approximation of the voltage gain is [1].

$$A_v \approx -g_m R_L \quad (6)$$

where g_m and R_L represents the effective load resistance. In practical RF circuits, however, finite output resistance, resonant loading, and frequency-dependent losses further shape the gain. A CG stage presents a resistive input [20],

$$Z_{in} \approx \frac{1}{g_m} \quad (7)$$

Consequently, a 50- Ω input termination can be approached by selecting,

$$g_m \approx \frac{1}{50} \approx 20 \text{ mS} \quad (8)$$

This direct g_m and input impedance linkage makes CG topologies attractive for broadband receivers, though achieving low noise, adequate gain, and good linearity at the same time typically requires noise-cancellation, feedback, or complementary-device techniques [5], [16].

2.4 Linearity Metrics: CMOS transistors exhibit nonlinear current-voltage and transconductance characteristics, which become particularly significant when the LNA is exposed to strong interferers or large input signals. For a weakly nonlinear amplifier, the input-output relationship can be represented using a polynomial approximation [1], [16], [20],

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \dots \quad (9)$$

where a_1 is the linear gain, the 2nd order coefficient a_2 generates IM2 products, and the 3rd order coefficient a_3 produces the close in IM3 products that fall near the wanted band [10], [20].

Consequently IIP2, IIP3, and P_{1dB} provide complementary measures, IIP2 characterizes 2nd order distortion, IIP3 extrapolates 3rd order linearity, and P_{1dB} marks the onset of large-signal compression in wideband systems these vary with center frequency and tone spacing [12], [10].

2.5 Figure of Merit: To compare designs across frequency and power levels, this review adopts the normalized FoM [3], [6]

$$FoM = \frac{G_{lin} \times IIP3_{mW} \times f_c (GHz)}{(F-1) \times P_{DC} (mW)} \quad (10)$$

where G_{lin} is the linear power gain, $IIP3_{mW}$ is the 3rd order input intercept point expressed in milliwatts, f_c is the centre frequency in GHz, F is the linear noise factor, and P_{DC} is the DC power consumption in mw.

FOM values are comparable only under consistent gain, IIP3, bandwidth, NF, and power conventions. Because measured silicon captures layout parasitic, passive quality factors, and packaging effects that schematic level simulation omits, this review weights experimentally validated results more heavily when assessing performance and technology trends [3], [6].

3. CMOS LNA Architectures

CMOS LNA architecture falls broadly into narrowband (NB) resonant topologies and wideband or reconfigurable topologies. NB designs exploit inductive resonance for high gain and less noise over a specific band, whereas wideband designs emphasize wide input matching, bandwidth extension, and robustness across multiple bands. Topology selection is therefore a fundamental design decision, since it directly sets the achievable NF, gain, linearity, bandwidth, power, voltage headroom, and silicon area. Table I summarizes the principal architectures and their typical strengths, limitations, and roles [3].

Table I : Comparison of Major CMOS LNA Architectures

Architecture	Primary benefit	Main limitation	Typical role
Common source	High gain; simple	Miller effect; bandwidth	NB/MB
Inductive-degenerated CS	Excellent noise/input matching	Inductors; NB	NB
Cascode CS	High gain; isolation	Voltage headroom	NB/MB
Common gate	Input 50-Ω match	NF can be higher	WB
Resistive feedback	WB, robust matching	Feedback noise, gain loss	WB
Noise-cancelling CG-CS	WB + low NF potential	Path matching/complexity	WB
Current reuse	High gain per current	Loading/headroom	WB
Complementary CMOS	Uses NMOS + PMOS gm	Mismatch/parasitic	WB
Inductor-less	Very small area	gain challenge	WB

*NB = Narrowband, WB = Wideband, MB = Medium band

The CS stage remains among the most widely used topologies owing to its high transconductance efficiency and simple implementation, though its bandwidth is constrained by parasitic capacitance and the Miller effect. Source degeneration particularly inductive degeneration improves the input impedance and adds a degree of freedom for simultaneous noise and input matching, making the inductively degenerated CS especially attractive for narrowband use [1]. The cascode configuration further raises reverse isolation and suppresses the Miller effect, but the stacked devices demand extra voltage headroom that becomes problematic as supply voltages scale down, limiting its suitability for low voltage operation [21].

By contrast, the CG stage presents an inherently low input impedance, $Z_{in} \approx 1/g_m$, enabling broadband 50- Ω matching and making CG topologies attractive for wideband and multiband receivers [5]. Conventional CG stages, however, exhibit a higher noise figure than optimized CS stages, motivating NC and complementary techniques [5], [21]. Resistive-feedback LNAs broaden bandwidth by reducing the frequency selectivity of resonant matching and improve tolerance to device and process variation, at the cost of added feedback noise and some gain reduction [14]. Noise-cancelling architectures, typically based on complementary CG/CS signal paths, tackle the fundamental trade-off between broadband input matching and noise: by summing multiple paths with appropriate amplitude and phase, the input-device noise is partially cancelled while the signal adds constructively though accurate path matching and added complexity are required [5] [6] [17] [22]. Current-reuse techniques improve power efficiency by sharing bias current across stacked transconductance stages, giving high gain per unit current for low-power receivers, but they are limited by internal loading, reduced signal swing, and constrained headroom in deeply scaled CMOS [6] [8].

Finally, inductor less LNAs remove large on chip inductors to save area and enable highly integrated broadband front ends, their main challenge is reproducing the noise, gain, selectivity, and linearity of inductive matching, which is why active feedback, noise cancellation, and g_m enhancement are commonly added [17] , [22]. Overall, no single architecture simultaneously optimizes noise figure, gain, linearity, bandwidth, power, and area; topology choice must instead follow the target application. Narrowband cellular and WLAN receivers favour resonant and inductively degenerated designs, whereas broadband 5G, multiband, and highly integrated receivers increasingly Favor CG, resistive-feedback, NC, complementary, current-reuse, and inductor less configurations [17]. This architecture-level trade-off sets the stage for the noise-reduction and linearity enhancement techniques discussed next.

3.1 Inductively Degenerated Common-Source LNA

The inductively degenerated CS LNA shown in Fig. 1 is one of the most established narrowband CMOS receiver architectures. A simplified small signal representation of input impedance (Z_{in}) can be written,

$$Z_{in} \approx s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s \quad (11)$$

where L_g = gate inductance, L_s = source degeneration inductance, C_{gs} = gate to source capacitance, At the operating frequency, where L_g resonates with the effective input capacitance, while L_s introduces a real term ($\omega_T \cdot L_s$) that enables a 50- Ω match without adding thermal noise, allowing a simultaneous noise and power match [3]. The topology offers low NF, high gain, good input matching, and predictable narrowband behavior, at the cost of on-chip inductors, added passive area, limited fractional bandwidth, and sensitivity to inductor Q. It therefore remains well suited to frequency-specific cellular, WLAN, and other narrowband front ends [1][15].

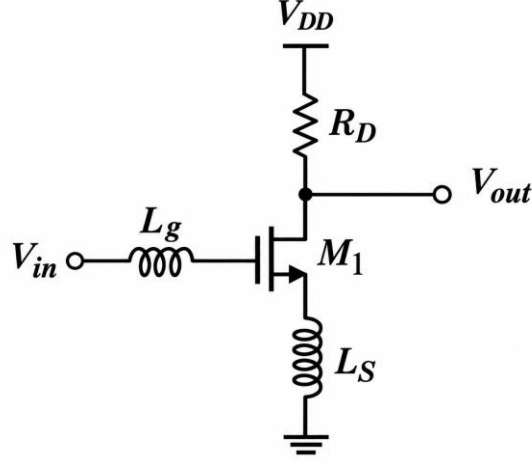


Fig.1 Inductively Degenerated Common Source Amplifier

3.2 Cascode LNA

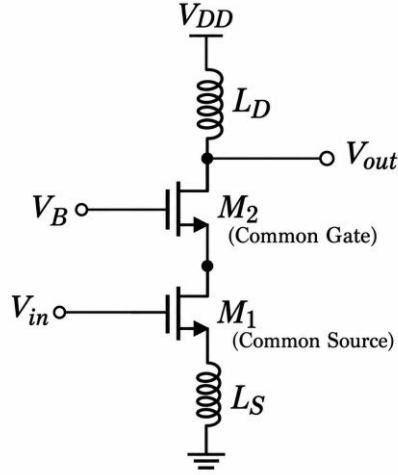


Fig.2 Cascode Amplifier

A cascode LNA incorporates a CG above the CS input transistor shown in Fig. 2. The upper device isolates the input transistor from the output node, thereby reducing reverse coupling and suppressing the Miller effect. The cascode configuration also increases the effective output resistance, which can improve voltage gain and output isolation. [13], [10].

The distribution of voltage swing between the stacked devices can further improve high-frequency operation by reducing the voltage variation experienced by the input transistor. These properties make the cascode structure attractive for high-gain RF front ends. The principal limitation is voltage headroom. Since multiple transistors are stacked between the supply rails, sufficient voltage must be available to maintain the devices in their intended operating regions. This becomes increasingly restrictive as supply voltages decrease with CMOS scaling. Therefore, cascode LNAs require careful biasing and signal-swing management in low-voltage designs [13].

3.3 Common-Gate LNA

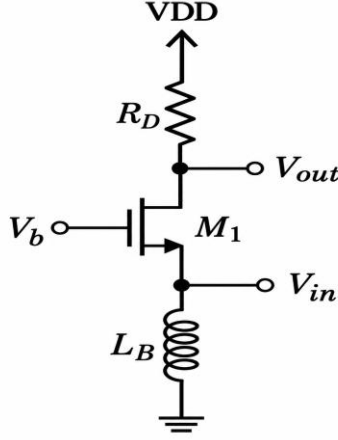


Fig.3 Common-Gate Amplifier

The CG topology show in Fig. 3 is particularly attractive for broadband operation because its input impedance (Z_{in}) can be written as,

$$Z_{in} \approx \frac{1}{g_m} \quad (12)$$

For a nominal $50\text{-}\Omega$ source,

$$g_m \approx \frac{1}{50} = 20 \text{ ms} \quad (13)$$

This removes the need for a highly selective resonant input-matching network and lets the CG stage cover a broad frequency range, making it widely investigated for broadband and multiband receivers [15][17]. The primary limitation is the trade-off among input matching, NF, gain, and power: increasing g_m improves matching but requires additional bias current. Consequently, g_m boosting, complementary device, current reuse, and NC techniques have been developed to improve the noise and power efficiency of CG-based LNAs [22].

3.4 Resistive-Feedback Amplifier

In Fig. 4, the resistive feedback LNA employs negative feedback to simultaneously regulate the voltage gain and input impedance over a wide frequency range. The resulting closed-loop voltage gain can be expressed as,

$$A_f = \frac{A}{1 + A\beta} \quad (14)$$

where A = open loop gain and β = feedback factor, for sufficiently large loop gain, feedback reduces the sensitivity of the response to device and passive-component variation and can extend the usable bandwidth, and it can provide broadband input matching without relying on high-Q inductors. The compromises are a closed-loop gain lower than the open-loop gain, added noise from the feedback network, and stability that must be verified across the full operating band. Resistive-feedback LNAs are therefore most effective when the bandwidth and matching gains justify the associated gain, noise, and stability penalties [23].

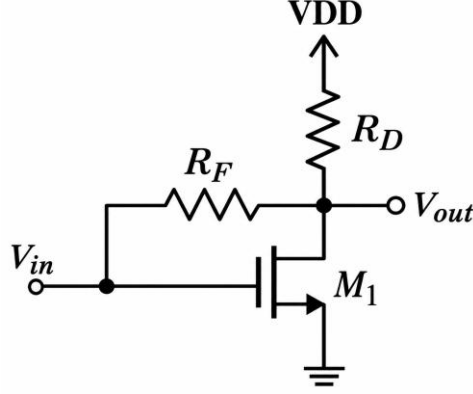


Fig.4 Resistive-Feedback Amplifier

4. Noise, Gain, Bandwidth, and Power-Reduction Techniques

The simultaneous optimization of noise figure, gain, bandwidth, and power is a central challenge in CMOS LNA design. Improving one metric often penalizes another increasing transconductance improves matching and gain but requires more bias current, while aggressive bandwidth extension can raise noise and reduce gain. A variety of circuit-level techniques have therefore been developed to improve overall performance without relying solely on higher power consumption. The following subsections summarize the principal techniques identified in the reviewed literature [6], [8].

4.1 g_m Boosting

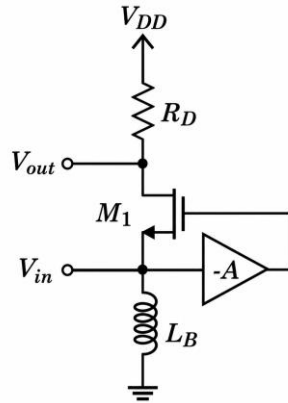


Fig. 5. g_m -Boosting Technique [6]

Transconductance enhancement, as illustrated in Fig. 5 and discussed in [6], is widely employed to improve input matching and gain efficiency in CMOS LNAs, particularly in common-gate and low-voltage architectures. In a generic g_m -boosted configuration, local feedback increases the effective transconductance, which can be approximately expressed as [6],

$$g_{m,eff} \approx (1 + A)g_m \quad (15)$$

where A = voltage gain of the auxiliary boosting path. The higher effective g_m allows the required input g_m to be met with a smaller intrinsic transistor, potentially reducing the bias current for a given input impedance especially useful in broadband LNAs that need a low input impedance over a wide range. However, the auxiliary stage adds noise, parasitic capacitance, stability concerns, and potential linearity degradation, so boosting must be optimized at the complete-circuit level rather than from its small-signal g_m enhancement alone [6], [22].

4.2 Current Reuse

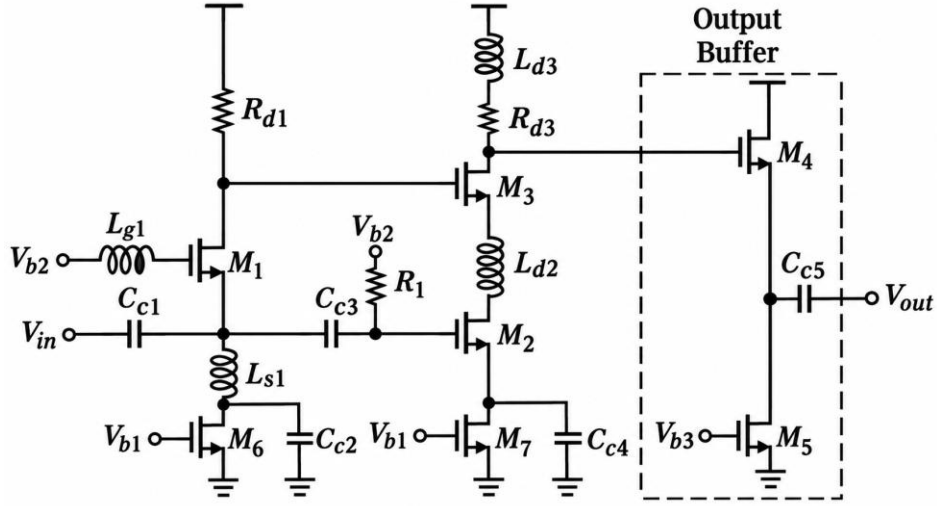


Fig. 6. Current-Reuse Technique [22]

Current-reuse techniques, as illustrated in Fig. 6 and discussed in [22], improve power efficiency by allowing multiple gain-producing devices or circuit stages to share a common bias current. Consequently, the required DC power consumption can be approximately expressed as [22],

$$P_{DC} = V_{DD}I_{bias} \quad (16)$$

sharing the bias current among several stages increases the achievable gain or signal-processing capability without a proportional rise in DC power [6]. This is particularly attractive for battery-powered, highly integrated receivers and can be combined with cascode, complementary, and noise-cancellation architectures to improve the gain-to-power ratio. The main limitation is the increased interaction among stacked or coupled devices: internal loading, reduced signal swing, limited headroom, and operating-region constraints grow more important as the supply drops, so current-reuse designs require careful biasing and large-signal analysis to ensure the efficiency gain does not degrade linearity or compression [22].

4.3 Body-Bias Techniques

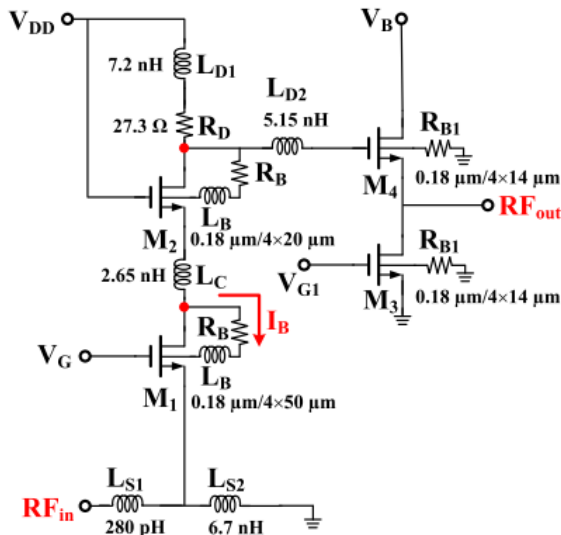


Fig. 7. Body - Biasing Technique [8]

Body-biasing techniques, as illustrated in Fig. 7 and discussed in [8], provide an additional degree of freedom for low-voltage CMOS LNA design. In the reported 3–9 GHz implementation, a high-resistance body-to-drain connection establishes the required DC body bias while maintaining an effectively floating body at RF frequencies. This allows the body potential to contribute to both the biasing and RF operation without requiring a conventional fixed-body connection [8].

At a 1-V supply, the LNA achieves approximately 3.3 mW DC power consumption, 10.7 dB gain, and 2.89 dB NF over 3–9 GHz. When the supply voltage is reduced to 0.8 V, the power consumption decreases to approximately 1.36 mW, while the NF increases to about 3.46 dB. These results demonstrate the potential of body-floating and self-biasing techniques for reducing supply voltage and power consumption. However, their impact on linearity, body-effect sensitivity, PVT variations, and bias stability must also be considered, since variations in body potential can alter the device operating point and nonlinear behaviour [8].

4.4 Low-Voltage g_m Enhancement

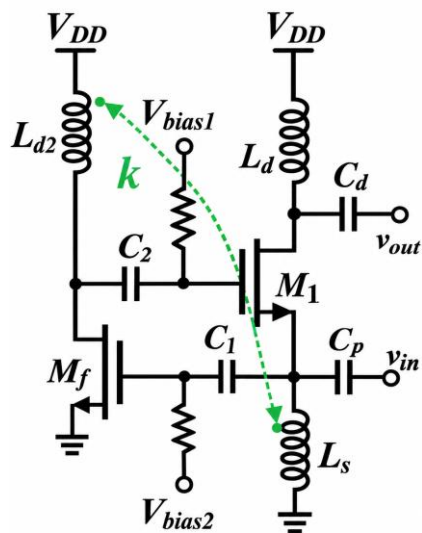


Fig. 8 Low-Voltage g_m Enhancement [6]

Low-voltage operation is increasingly important in scaled CMOS technologies; however, reducing the supply voltage directly limits the available voltage headroom and signal swing, resulting in a fundamental trade-off between low power consumption and large-signal linearity [6]. As illustrated in Fig. 8, the reported 0.5-V CMOS LNA employs active and passive g_m -enhancement techniques within an enhanced folded-cascode architecture to maintain adequate gain and bandwidth at an extremely low supply voltage. The design achieves approximately 14.5 dB gain, 3.2 dB NF, a 3-dB bandwidth of 5.3–6.4 GHz, and 0.88 mW DC power consumption, with an IIP3 of approximately -15.9 dBm at 5.8 GHz [6]. These results highlight the inherent trade-offs associated with low-voltage LNA design. Although g_m -enhancement techniques can maintain useful gain and noise performance under reduced supply voltage, the limited voltage swing increases susceptibility to distortion and compression. The relatively low IIP3 further indicates that power and noise optimization at low supply voltages must be considered together with linearity and dynamic-range requirements [6] [8].

Overall, these techniques show that modern CMOS LNA optimization increasingly relies on co-design rather than single-parameter optimization. g_m boosting, current reuse, complementary operation, body engineering, and low-

voltage circuit techniques can each improve gain, noise, bandwidth, or power efficiency, but each adds circuit-level trade-offs interactions that become critical when both low NF and high linearity are required over a wide band, motivating the treatment of nonlinear behavior and linearization in the following sections [6] [8] [22] [16] [17].

5. Linearity and Distortion in CMOS LNAs and Detailed Review of Linearity-Improvement Techniques

Linearity is critical because the LNA must amplify weak signals while remaining linear against strong blockers, adjacent-channel interferers, and transmitter leakage; a linear LNA limits in-band and out-of-band intermodulation and preserves receiver dynamic range [2], [24]. Expanding the MOS drain current about its operating point gives,

$$i_d \approx g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \dots \quad (17)$$

where g_1 , g_2 , and g_3 are the 1st, 2nd, and 3rd order nonlinear coefficients. Distortion arises mainly from nonlinear transconductance (g_m) and output conductance (g_{ds}) the latter becoming significant when the drain-source voltage swings widely under large signals[2], [24]. For a two-tone input,

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \quad (18)$$

the 2nd order term produces components at $2f_1$, $2f_2$, f_1+f_2 , and $|f_1-f_2|$, while the 3rd order term yields the critical IM3 products $2f_1-f_2$ and $2f_2-f_1$. IM3 products are troublesome because they fall close to the wanted signal and cannot be filtered out. Second-order distortion is also not always independent: through feedback, device interaction, and frequency-dependent loading, IM2 components can fold into third-order distortion an important consideration for high-linearity design[4] [24].

5.1 IIP2, IIP3, and P_{1dB}

LNA linearity has traditionally been captured by IIP3, since 3rd order products dominate close in intermodulation in narrowband receivers. In broadband/direct-conversion architectures, however, 2nd order products can land in-band or fold to low frequencies, making IIP2 equally important [25] [16]. The three metrics are complementary, IIP2 gauges 2nd order distortion, IIP3 extrapolates 3rd order performance, and P_{1dB} marks ~1 dB gain compression. Because a high IIP3 need not imply good compression, nor a high P_{1dB} low close-in IM3, all three should be weighed together with NF, gain, bandwidth, and power [1][24] [26].

5.2 Two-Tone Spacing and Frequency Dependence

Reporting linearity at a single frequency and fixed tone spacing is often inadequate for broadband receivers, where the nonlinear response depends on both operating frequency and tone separation [2]. A more appropriate representation is

$$IIP3 = IIP3(\Delta f), \quad IIP2 = IIP2(\Delta f) \quad (19)$$

$$P_{1dB} = P_{1dB}(f_c) \quad (20)$$

where f_c is the center frequency and Δf is the two-tone spacing. Reactive matching, parasitics, feedback, and frequency dependent device parameters introduce memory effects and phase shifts, so upper and lower IM3 amplitudes can differ and the optimum cancellation condition shifts with frequency and spacing, a technique tuned at one frequency may underperform elsewhere in the band [2].

5.3 Classification of Linearization Techniques

The reviewed literature can be organized into different categories (a)Feedback linearization (b)Feedforward linearization (c) Derivative superposition (DS) including modified and complementary DS (CDS) (d) Noise / distortion cancellation (e) post-distortion. These are not mutually exclusive, recent designs often combine two or more to address different distortion sources or offset the limits of a single method. The following subsections review each

by operating mechanism, achievable improvement, and associated noise, power, bandwidth, and implementation trade-offs.

- (a) **Feedback Linearization:** Negative feedback is one of the most fundamental approaches to improving amplifier linearity by reducing the closed loop sensitivity to nonlinear variations in the forward path, it suppresses the effective nonlinear gain shown in Fig. 9. Consider a weakly nonlinear amplifier with linear gain g_1 and 2nd and 3rd order coefficients g_2 and g_3 , placed in a loop with linear feedback factor β , and define the linear open-loop gain $T_0 = g_1\beta$.

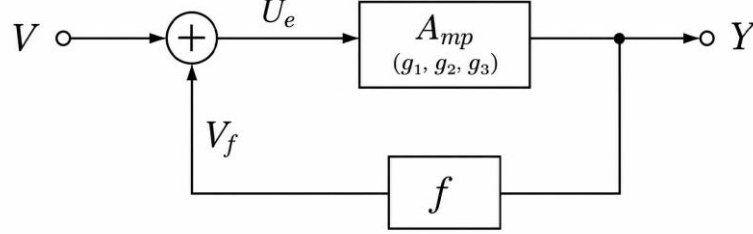


Fig.9 Nonlinear amplifier with negative feedback

The closed-loop response is then a third-order power series [1], [26]

with closed-loop coefficients,

$$b_1 = \frac{g_1}{(1+T_0)}, b_2 = \frac{g_2}{(1+T_0)^3}, b_3 = \frac{1}{(1+T_0)^4} \left[g_3 - \frac{2g_2^2}{g_1} \frac{T_0}{(1+T_0)} \right]$$

The resulting input intercept points of the closed-loop system are,

Equation (22) shows that feedback improves IIP2 by a factor of $(1+T_0)$, and (23) shows it improves IIP3 by $(1+T_0)^{3/2}$ but only when $g_2 \approx 0$. When $g_2 \neq 0$ and g_1 and g_3 have opposite signs, as they do for typical MOSFET bias, the bracketed denominator in eq. (23) shrinks and AIIIP3,cl degrades. In this mechanism, called 2nd order interaction, the intrinsic 2nd order nonlinearity folds into 3rd order distortion through the loop, so whenever an amplifier is placed in feedback its IM3 arises from two sources: the intrinsic 3rd order term and the fed back 2nd order term [11]. Because the offending product is an odd-order term, it is not rejected by a differential topology; harmonic termination and IM2 injection can suppress it, but both are narrowband and therefore unsuitable for wideband linearization [4], [11]. In CMOS LNAs the practical improvement is thus doubly constrained: the loop gain T_0 needed to enhance IIP2 and IIP3 is bounded by the LNA's gain, noise, and power budgets, and the residual second-order interaction limits the achievable IIP3 [1]. Feedback consequently provides useful broadband impedance control and modest linearization but is generally insufficient as a stand-alone means of simultaneously optimizing NF, gain, bandwidth, and linearity which motivates the harmonic-termination and derivative-superposition techniques discussed next [12], [26]

- (b) **Feedforward Linearization:** The technique uses a main amplifier and an auxiliary amplifier to generate and cancel nonlinear distortion. As shown in Fig. 10, the input X is directly applied to the main amplifier, while a scaled version pX is applied to the auxiliary amplifier. The auxiliary output is subsequently scaled by p^n and subtracted from the main-amplifier output.

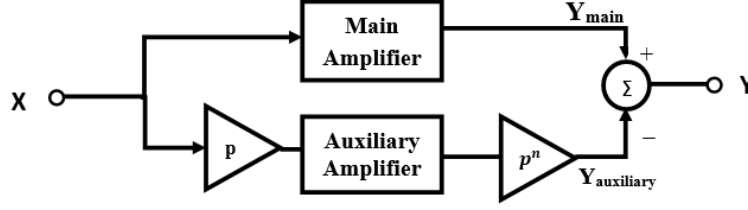


Fig. 10: Basic Concept of Feedforward Linearization Technique

Assuming both amplifiers exhibit the same weakly nonlinear characteristics,

$$Y_{main} = g_1X + g_2X^2 + g_3X^3 \quad (24)$$

and the auxiliary-path output is

$$Y_{aux} = p^n[g_1(pX) + g_2(pX)^2 + g_3(pX)^3] \quad (25)$$

Thus, the overall output after subtraction is

$$Y = g_1(1 - p^{n+1})X + g_2(1 - p^{n+2})X^2 + g_3(1 - p^{n+3})X^3 \quad (26)$$

By appropriately selecting p and n , the auxiliary path can be made to produce a distortion component with equal amplitude and opposite phase to that of the main path, thereby cancelling the targeted nonlinear term. A single auxiliary path can primarily suppress one dominant distortion order, whereas multiple auxiliary paths can be employed for simultaneous cancellation of IM2 and IM3[10]. The principal advantage of this approach is effective distortion cancellation without requiring high intrinsic linearity from the main amplifier. However, the technique requires additional power, area, and noise, and its performance is sensitive to amplitude and phase mismatch between the main and auxiliary paths. These limitations make feedforward linearization less attractive for compact, broadband CMOS LNAs and motivate lower-complexity techniques such as derivative superposition and IM2-injection linearization.[11]

- (c) **Derivative Superposition:** DS is a device level linearization technique that exploits the nonlinear characteristics of transistors biased in different operating regions. A main NMOS transistor M_1 , typically biased in strong inversion, is combined in parallel with an auxiliary NMOS transistor M_2 , biased in weak inversion as shown in figure. 11. Since their 3rd order transconductance coefficients can have opposite signs, the effective 3rd order coefficient is,

$$g_{3,tot} = g_{3,M1} + g_{3,M2} \quad (27)$$

By appropriately selecting the device dimensions and bias conditions,

$$g_{3,M1} \approx -g_{3,M2} \quad (28)$$

resulting in

$$g_{3,tot} \approx 0 \quad (29)$$

DS yields a significant IIP3 improvement without a large auxiliary path or major power penalty [15] [27]. However, since g_2 is positive for transistors in moderate or strong inversion, DS improves IIP3 while worsening IIP2; it does not improve P_{1dB}, and the range of zero $g_{3,tot}$ is narrow. Cancellation also holds only over a finite range, since mismatch, PVT variation, parasitics, and operating region changes shift the cancellation point; at RF, 2nd order interaction through the degeneration inductance further limits the achievable IIP3, which the modified-DS method addresses by tuning two series source-degeneration inductors so the composite third-order contribution opposes the 2nd order term [27].

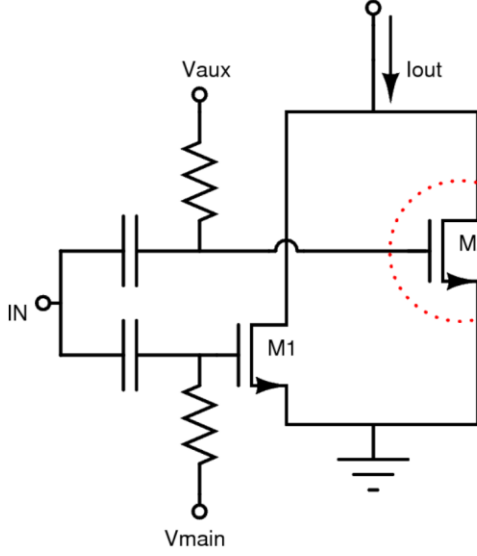


Fig. 11 DS configuration [10]

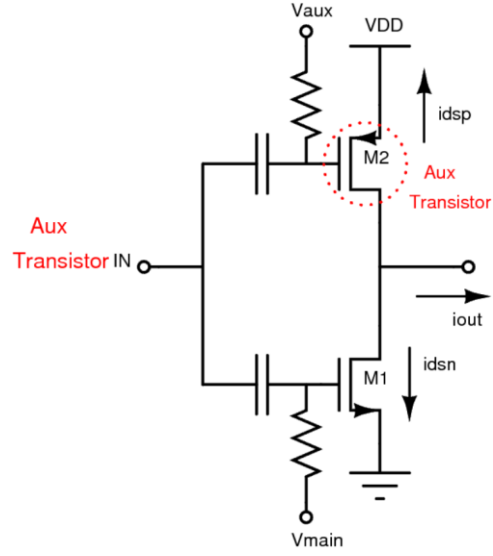


Fig. 12 CDS configuration[10]

Complementary derivative superposition (CDS) extends DS by combining NMOS and PMOS devices in a complementary push-pull configuration as shown in figure 12. This arrangement can provide both even and odd distortion cancellation while avoiding the need for an external balun. For complementary devices subjected to opposite-phase signals, the drain currents can be expressed as

$$i_{dsn} = g_{1n}V_{gs} + g_{2n}V_{gs}^2 + g_{3n}V_{gs}^3, \quad (30) \quad i_{dsp} = -g_{1p}V_{gs} + g_{2p}V_{gs}^2 - g_{3p}V_{gs}^3. \quad (31)$$

Their differential combination produces

$$i_{out} = (g_{1n} + g_{1p})V_{gs} + (g_{2n} - g_{2p})V_{gs}^2 + (g_{3n} + g_{3p})V_{gs}^3. \quad (32)$$

The complementary arrangement raises the total transconductance, reduces the IM2 term (because g_{2n} and g_{2p} subtract), and reduces the IM3 term, so CDS improves IIP3 without degrading IIP2 unlike conventional DS [16]. Because IIP2 and IIP3 do not share the same optimum bias, (32) allows either optimum IIP3 or optimum IIP2, but not both. Practical variants use separate NMOS/PMOS body bias to shift the g_3 profiles for optimum cancellation, auxiliary NMOS/PMOS pairs biased across saturation and triode for large-signal (P_{1dB}) linearization, and current-based or source-degenerated biasing with a series battery to relax the strong PVT sensitivity of the cancellation[16].

- (d) **Noise / Distortion cancellation:** NC Method reduces the conventional trade-off between NF and source-impedance matching, enabling a low-NF and well-matched LNA [5], [10], [11], [17][10], [11], [17]. As shown in Fig. 13, the generalized NC architecture consists of three stages: input matching, noise/distortion cancellation, and output combining. The main path generally employs a CS stage with resistive feedback or a parallel CG-CS topology, while an auxiliary path senses the signal and noise associated with the matching transistor. The two paths are combined such that the noise and distortion components cancel, while the desired signal adds constructively [10], [11], [15], [17].

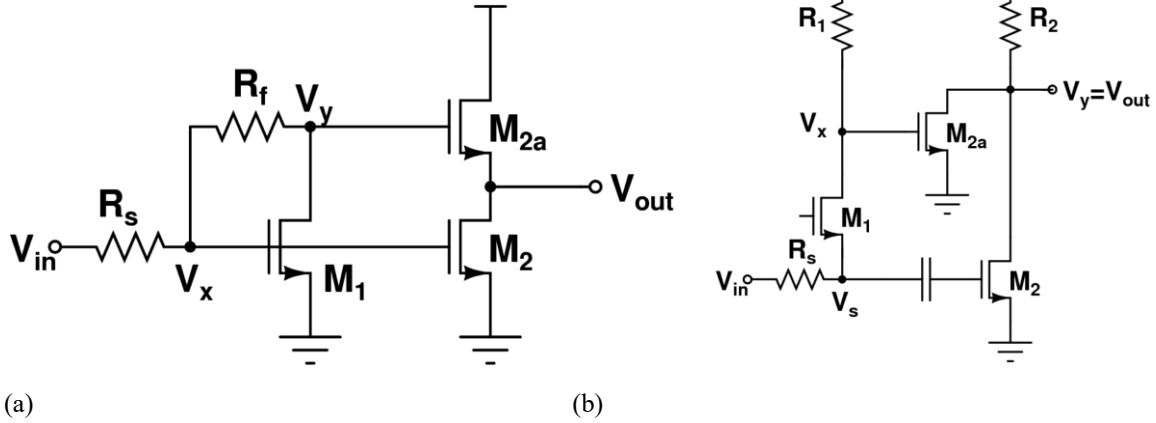


Fig. 13 NC implementations based on (a) CS with resistive feedback, (b) CG with differential output [10]

The CS resistive-feedback implementation shown in Fig. 13(a), M_1 provides input matching through R_f , while M_2 and M_{2a} form the auxiliary cancellation path. The cancellation condition is obtained by making the sensing node voltages approximately equal,

$$V_x = V_y \quad (33)$$

with the corresponding design relationships given by,

$$g_{1,M1}R_S = g_{1,M2}(R_F + R_S) \quad (34) \quad g_{1,M1}R_1 = g_{1,M2}R_2 \quad (35) \quad g_{1,M2}R_S = g_{1,M2a}R_1 \quad (36)$$

These conditions ensure that the noise and nonlinear components generated by the matching transistor reach the output through the two paths with appropriate amplitude and phase for cancellation, while the desired signal components add constructively [10]. The CG implementation shown in Fig. 13(b) provides broadband input matching. Since the noise and nonlinear current of the matching transistor depend on both V_{GS} and V_{DS} , NC can suppress both g_m and g_{ds} related nonlinearities, unlike techniques that primarily address g_m nonlinearity [5], [10], [11], [15], [17]. The residual distortion is mainly determined by the auxiliary path, including its intrinsic third-order distortion and the second-order interaction associated with the CG-CS cascade [5]. Several approaches have been reported to improve NC linearity, including optimum biasing, CDS and multi-path cancellation [4], [5], [10], [11], [16], [17], [24], [25]. Earlier techniques generally focused on improving either IIP2 or IIP3, whereas combined approaches enable simultaneous suppression of even and odd order distortion [24], [25]. The three-path NC architecture in [4], [5], [10], [11], [16], [17], [24], [25]. extends the bandwidth to 1–20 GHz and provides additional IIP3 enhancement, although simultaneous broadband IIP2 improvement remains challenging. Therefore, combining NC with CDS/DS, complementary devices, feedback, and additional cancellation paths remains a promising approach for achieving simultaneous improvement in NF, bandwidth, and linearity.

- (e) **Post-Distortion:** Post-distortion introduces a nonlinear auxiliary circuit after the principal gain stage shown in Fig. 14. The auxiliary device senses the amplified signal and generates a nonlinear current or voltage designed to compensate for the distortion produced by the main amplifier. In contrast to input side linearization, post-distortion reduces the direct loading of the input matching network and can therefore provide greater flexibility in preserving the LNA's input noise and matching characteristics. Appropriate biasing of the auxiliary nonlinear device can produce a compensating third-order component without significantly disturbing the small-signal gain path[28].

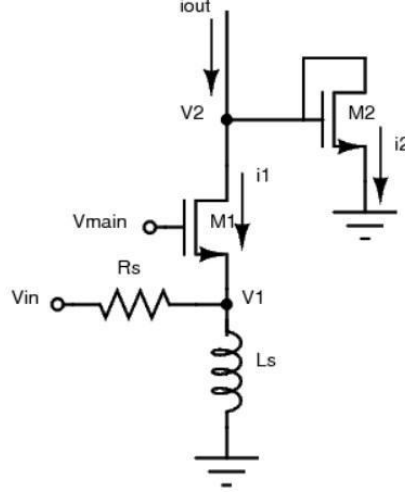


Fig. 14 Conceptual post-distortion implementation [10].

Post-distortion (PD) adds an auxiliary transistor at the output of the main device that replicates and cancels its nonlinear drain current, with minimal impact on input matching and all devices in saturation for robust cancellation [9], [28]. The nonlinear currents are

$$i_1 = g_{1,M1}v_1 + g_{2,M1}v_1^2 + g_{3,M1}v_1^3 \quad (37)$$

$$i_2 = g_{1,M2}v_2 + g_{2,M2}v_2^2 + g_{3,M2}v_2^3 \quad (38)$$

with v_2 related to v_1 by $v_2 = b_1v_1 - b_2v_1^2 - b_3v_1^3$, so the combined output current is

$$\begin{aligned} i_{out} = & (g_{1,M1} - b_1g_{1,M2})v_1 + (g_{2,M1} - b_1^2g_{2,M2} - b_2g_{1,M2})v_1^2 \\ & + (g_{3,M1} - b_1^3g_{3,M2} - g_{1,M2}b_3 - 2g_{2,M2}b_1b_2)v_1^3 \end{aligned} \quad (39)$$

PD partially cancels both 2nd and 3rd order terms and, unlike DS, improves both IIP2 and IIP3, at a modest gain/NF/power penalty since M_2 is designed more nonlinear than M_1 [9]. Its limitations are the direct dependence of the auxiliary transistor on the main-transistor current and the difficulty of matching NMOS/PMOS pairs across PVT; post-distortion star feedback variants relax this by driving the auxiliary input from different circuit nodes [9], [28].

5. Recent Sub-6 GHz LNA Developments

Recent sub-6 GHz CMOS LNA implementations reveal several recurring design directions aimed at meeting the simultaneous demands of low noise, high gain, broadband operation, low power, and improved linearity g_m enhancement, NC, DS, CDS, inductor less implementation and post distortion. Rather than improving one parameter in isolation, recent designs increasingly combine several techniques for a more balanced result [6],[9],[15], [16],[17],[21], [22],[23], [28], [29].

A broadband linearity cannot be captured by a single IIP3 figure. A broadband receiver simultaneously handles multiple channels, adjacent-channel interferers, out-of-band blockers, and transmitter leakage, so linearity is more faithfully expressed as a frequency and spacing dependent quantity, $IIP3(f_c, \Delta f)$, $IIP2(f_c, \Delta f)$, and $P_{1dB}(f_c)$, where f_c is the centre frequency and Δf the two-tone spacing [10]. Reactive matching, parasitic, feedback, and frequency dependent loading introduce memory effects that make the upper and lower side IM3 components unequal and shift the optimum cancellation condition with frequency and spacing, a technique that improves IIP3 strongly at one setting may help far less elsewhere in the band. Broadband linearization must therefore be treated as a frequency dependent problem rather than a single point optimization.

Table II. Representative Recent Sub-6 GHz CMOS LNA Implementations

Ref..	Tech (nm)	Technique	Freq. (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Area (mm ²)
[6], 2023	180	Enhanced folded cascode, active/passive g_m improve	5.3–6.4	14.5	3.2	−15.9	0.88	0.42
[8], 2021	180	Body-floating and self-bias	3–9	9.4	3.46	NR	1.36	NR
[9], 2013	180	Post distortion technique	1.6-9.7	9.6-12.6	3.9-5.8	9	10.6	NR
[16], 2017	180	NC mechanism + Multiple complementary NMOS & PMOS configurations	0.1- 2	17.5	2.9-3.5	10.6-14.3	21.34	NR
[17], 2020	65	Triple-path noise-cancellation	1-20	12.8	3.3-5.3	2.2-6.8	20.3	0.096
[21], 2008	350	Capacitive cross-coupling	2.2	8.4	1.92	-2.55	16.2	NR
[22], 2018	180	Current reuse feed-forward noise cancelation	2-5	13	6	NR	10.8	NR
[23], 2019	65	Resistor feedback and source follower feedback	0.5-7	16.8	3.3 ± 0.45	NR	13.56	0.044
[28], 2021	65	Post distortion star feedback	3-10.6	11.2	3.2	24	15	0.874

**NR denotes a value not reported.*

Table II highlights clear trade-offs among bandwidth, gain, NF, IIP3, power, and area across recent sub-6 GHz CMOS LNAs. The g_m -enhanced design in [6] achieves the lowest reported power (0.88 mW) with 14.5-dB gain and 3.2-dB NF over 5.3–6.4 GHz, but its IIP3 of −15.9 dBm reflects limited linearity. By contrast, the post-distortion design in [9] provides a much wider 1.6–9.7-GHz bandwidth and 9 dBm IIP3, at the expense of higher NF (3.9–5.8 dB) and lower gain. Noise-cancellation approaches show strong broadband capability: [17] spans 1–20 GHz with 12.8-dB gain and 3.3–5.3-dB NF in only 0.096 mm², though its IIP3 of 2.2–6.8 dBm and 20.3-mW power reveal a bandwidth, linearity & power trade-off, while the complementary noise-cancellation design in [16] reaches higher gain (17.5 dB), lower NF (2.9–3.5 dB), and 10.6–14.3-dBm IIP3 at the cost of 21.34 mW. The feedback-based design in [22] combines a 0.5–7-GHz bandwidth, 16.8-dB gain, 3.3 ± 0.45 -dB NF, and a very small 0.044-mm² area, though its IIP3 is not

reported. The strongest reported linearity comes from the post-distortion star-feedback architecture in [28], with 24-dBm IIP3 over 3–10.6 GHz at 11.2-dB gain, 3.2-dB NF, and 15 mW, albeit in a comparatively large 0.874 mm². Overall, low-power techniques favour power efficiency, noise-cancellation techniques favour NF and bandwidth, feedback techniques favour compact broadband implementation, and post-distortion techniques deliver the strongest linearity; no single architecture is best in every metric, which motivates hybrid approaches that combine noise cancellation, g_m enhancement, feedback, and distortion linearization to obtain a balanced broadband LNA [1].

6. Research Gaps and Future Research Directions

Despite clear progress in noise, bandwidth, power efficiency, and linearity, no design yet achieves low NF, high linearity, wide bandwidth, low power, small area, and PVT robustness at once. The principal gaps follow.

- Joint NF - linearity optimization: low NF and high IIP3 remain hard to obtain together, motivating co-optimization at the transistor, circuit, and receiver levels [6], [8].
- Broadband IIP2/IIP3 characterization: IIP2 is under-reported; reporting IIP2 and IIP3 over multiple frequencies and tone spacings would better represent robustness [1], [24].
- Robust and adaptive linearization: most techniques cancel best only at a specific bias/frequency/power/spacing, motivating adaptive, digitally assisted linearization with PVT-aware calibration [15] [23].
- Low-overhead broadband post-distortion: co-optimized for gain, phase, bandwidth, and power, combined with complementary or noise-cancelling structures [9], [28].
- Beyond g_m : g_{ds} and cross-term effects, requiring multidimensional device models rather than a one-dimensional $id(v_{gs})$ element, especially at low supply [2].
- Low-voltage operation and dynamic range: architectures that distribute voltage swing and sustain P_{1dB} and IIP3 without raising VDD [6], [8].
- Inductorless broadband performance: reproducing inductive matching actively without excessive noise, power, or stability penalties [16], [24].
- Advanced CMOS and FD-SOI: integrating body-bias control with circuit-level linearization and noise cancellation [8], [17].
- Phase-aligned broadband cancellation: co-designing matching, signal paths, auxiliary distortion generators, and loading to hold the vector relationship across the band [14], [16], [18],
- AI-assisted design: machine-learning-assisted optimization and surrogate modelling over the coupled design space, validated in silicon.
- Reconfigurable 5G/Wi-Fi front ends: gain bypass, multiband matching, bandwidth control, and adaptive linearization without excessive parasitic or area [12].
- Joint LNA-mixer and receiver-level optimization, so an individual metric is not over-optimized for little receiver-level benefit [8] [28].
- Reporting and reproducibility: consistent, complete reporting of technology, power, bandwidth definition, S-parameters, NF vs. frequency, IIP2/IIP3/ P_1 dB with tone conditions, measured/simulated status, area, FoM definition, and robustness [1], [7].

The overarching challenge is not maximizing IIP3 or minimizing NF alone, but maintaining a balanced set,

$$\{NF, G, IIP2, IIP3, P_{1dB}, BW, P_{DC}, A_{core}\} \quad (31)$$

under realistic PVT, mismatch, parasitic, and blocker conditions which with consistent measurement practice, matters more than any single figure of merit [27] [31].

7. Conclusion

This article has reviewed sub-6 GHz CMOS LNA design, extending both architectures and linearization techniques. Inductively degenerated CS and cascode topologies remain attractive for narrowband use, while common-gate, resistive-feedback, noise-cancelling, complementary, current-reuse, and inductor less architectures suit broadband and multiband operation. The reviewed linearization methods feedback, feedforward, DS/CDS, noise/distortion cancellation, and post-distortion. Each tackle device nonlinearity differently but trade off against noise, power, bandwidth, headroom, parasitic, and PVT sensitivity. For broadband LNAs, IIP3 alone is insufficient: IIP2, IIP3, and P_{1dB} should be assessed across frequency and tone spacing, together with g_{ds} effects, g_m & g_{ds} cross terms, parasitic coupling, and memory effects. The next generation will need low voltage, low power, broadband, PVT robust designs that hold low NF and high linearity together through hybrid NC, phase aligned linearization, adaptive and body bias techniques, AI assisted optimization, and LNA+ Mixer design, evaluated by a balanced set of experimentally validated metrics rather than a single FoM.

REFERENCES

1. B. Ellis, *The Design of CMOS Radio-frequency Integrated Circuits*, 2nd ed., vol. 16, no. 2. Cambridge, UK ; Cambridge University Press, 2004.
2. R. A. Baki, T. K. K. Tsang, and M. N. El-Gamal, "Distortion in RF CMOS short-channel low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 46–55, Jan. 2006, doi: 10.1109/TMTT.2005.860897.
3. M. K. Bouchoucha, M. Coustans, M. J. Barragan, A. Cathelin, and S. Bourdel, "Performance benchmark of State-of-the-art Sub-6-GHz wideband LNAs Based on an Extensive Survey," in *Proceedings - IEEE International Symposium on Circuits and Systems*, May 2023, vol. 2023-May, pp. 1–5, doi: 10.1109/ISCAS46773.2023.10181964.
4. S. Lou and H. C. Luong, "A linearization technique for RF receiver front-end using second-order-intermodulation injection," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2404–2412, Nov. 2008, doi: 10.1109/JSSC.2008.2004531.
5. C. F. Liao and S. I. Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007, doi: 10.1109/JSSC.2006.889356.
6. G. Feng, L. Zheng, Y. Wang, and Q. Xue, "A 0.5-V 0.88-mW Low Noise Amplifier With Active and Passive G_m Enhancements in Sub-6 GHz Band," *IEEE Microw. Wirel. Technol. Lett.*, vol. 33, no. 8, pp. 1159–1162, Aug. 2023, doi: 10.1109/lmwt.2023.3276915.
7. M. Kumar, "A UWB LNA with cascade of CCG and CS stage with improvement in gain and noise in 90-nm technology," *Mater. Today Proc.*, 2023, doi: 10.1016/j.matpr.2023.03.355.
8. J. F. Chang and Y. S. Lin, "3-9-GHz CMOS LNA Using Body Floating and Self-Bias Technique for Sub-6-GHz 5G Communications," *IEEE Microw. Wirel. Components Lett.*, vol. 31, no. 6, pp. 608–611, Jun. 2021, doi: 10.1109/LMWC.2021.3075279.
9. B. Guo and X. Li, "A 1.6-9.7 GHz CMOS LNA linearized by post distortion technique," *IEEE Microw. Wirel. Components Lett.*, vol. 23, no. 11, pp. 608–610, Nov. 2013, doi: 10.1109/LMWC.2013.2281426.
10. N. K. Patel and H. P. Koringa, "Systematic Analysis of Linearization Techniques for Wideband RF Low-Noise Amplifier," in *Lecture Notes in Electrical Engineering*, 2023, vol. 962, pp. 27–44, doi: 10.1007/978-981-19-6780-1_3.
11. H. Zhang and E. Sánchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 58, no. 1, pp. 22–36, 2011, doi: 10.1109/TCSI.2010.2055353.
12. E. A. Keehr and A. Hajimiri, "Equalization of third-order intermodulation products in wdeband direct conversion receivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2853–2867, 2008, doi: 10.1109/JSSC.2008.2005701.
13. V. Aparin and C. Persico, "Effect of out-of-band terminations on intermodulation distortion in common-emitter circuits," *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 3, pp. 977–980, 1999, doi: 10.1109/mwsym.1999.779549.
14. V. Aparin and L. E. Larson, "Linearization of monolithic LNAs using low-frequency low-impedance input termination," in *European Solid-State Circuits Conference*, 2003, pp. 137–140, doi: 10.1109/ESSCIRC.2003.1257091.
15. B. Kim, J. S. Ko, and K. Lee, "Highly linear CMOS RF MMIC amplifier using multiple gated transistors and its Volterra series analysis," *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 3, pp. 515–518, 2001, doi: 10.1109/MWSYM.2001.966944.
16. B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A Wideband Noise-Canceling CMOS LNA with Enhanced Linearity by Using Complementary nMOS and pMOS Configurations," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1331–1344, May 2017, doi: 10.1109/JSSC.2017.2657598.
17. H. Yu, Y. Chen, C. C. Boon, P. I. Mak, and R. P. Martins, "A 0.096-mm² 1-20-GHz triple-path noise-canceling common-gate common-source LNA with dual complementary pMOS-nMOS configuration," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 1, pp. 144–159, Jan. 2020, doi: 10.1109/TMTT.2019.2949796.
18. R. Paulin, P. Cathelin, G. Bertrand, A. Monroy, J. Morelle, and T. Schwartzmann, "A 12.7dBm IIP3, 1.34dB NF, 4.9GHz-5.9GHz 802.11a/n LNA in 0.13 μ m PD-SOI CMOS with Body-Contacted transistor," in *IEEE MTT-S International Microwave Symposium Digest*, May 2016, vol. 2016-Augus, pp. 1–3, doi: 10.1109/MWSYM.2016.7540301.

19. R. Van De Beek, J. Bergervoet, H. Kundur, D. Leenaerts, and G. Van Der Weide, "A 0.6-to-10GHz receiver front-end in 45nm CMOS," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2008, vol. 51, pp. 128–601, doi: 10.1109/ISSCC.2008.4523090.
20. T. W. Kim, "A common-gate amplifier with transconductance nonlinearity cancellation and its high-frequency analysis using the volterra series," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 1, pp. 1461–1469, Jun. 2009, doi: 10.1109/TMTT.2009.2019998.
21. X. Fan, H. Zhang, and E. Sánchez-Sinencio, "A noise reduction and linearity improvement technique for a differential cascode LNA," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 588–599, Mar. 2008, doi: 10.1109/JSSC.2007.916584.
22. A. R. A. Kumar, B. D. Sahoo, and A. Dutta, "A wideband 2-5 GHz noise canceling subthreshold low noise amplifier," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 7, pp. 834–838, Jul. 2018, doi: 10.1109/TCSII.2017.2719678.
23. H. Yu, Y. Chen, C. C. Boon, C. Li, P. I. Mak, and R. P. Martins, "A 0.044-mm² 0.5-To-7-GHz Resistor-Plus-Source-Follower-Feedback Noise-Cancelling LNA Achieving a Flat NF of 3.3±0.45 dB," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 1, pp. 71–75, Jan. 2019, doi: 10.1109/TCSII.2018.2833553.
24. T. W. Kim, B. Kim, and K. Lee, "Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 223–229, Jan. 2004, doi: 10.1109/JSSC.2003.820843.
25. A. Vaghela and H. Koringa, "Advances in active down-conversion mixer linearity techniques: a comprehensive review," *Discov. Electron.*, vol. 1, no. 1, p. 3, 2024, doi: 10.1007/s44291-024-00004-3.
26. J. S. Fairbanks and L. E. Larson, "Analysis of optimized input and output harmonic termination on the linearity of 5 GHz CMOS radio frequency amplifiers," in *Proceedings - 2003 IEEE Radio and Wireless Conference, RAWCON 2003*, Aug. 2003, pp. 293–296, doi: 10.1109/RAWCON.2003.1227950.
27. V. Aparin, G. Brown, and L. E. Larson, *Linearization of CMOS LNA'S VIA optimum gate biasing*, vol. 4, 2004.
28. S. Veisi and M. Yargholi, "Design of a high linear and ultra-wideband LNA using post distortion star feedback method," *Microelectronics J.*, vol. 107, p. 104949, 2021, doi: 10.1016/j.mejo.2020.104949.
29. R. Zhou, S. Liu, J. Liu, Y. Liang, and Z. Zhu, "A 0.1-3.5-GHz Inductorless Noise-Canceling CMOS LNA with IIP3 Optimization Technique," *IEEE Trans. Microw. Theory Tech.*, vol. 70, no. 6, pp. 3234–3243, Jun. 2022, doi: 10.1109/TMTT.2022.3161279.
30. L. Vimalan and S. Devi, "Performance analysis of various topologies of common source low noise amplifier (CS-LNA) at 90nm Technology," *2018 3rd IEEE Int. Conf. Recent Trends Electron. Inf. Commun. Technol. RTEICT 2018 - Proc.*, pp. 1687–1691, 2018, doi: 10.1109/RTEICT42901.2018.9012326.
31. L.-C. Wang, Vincent W.S. Wong, R. Schober, and Derrick Wing Kwan Ng, *Key Technologies for 5G Wireless Systems*, 1st ed.: Cambridge University Press, 2017.