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Article

A Pipelined Fixed-Point FPGA Architecture for Binary Antilogarithmic Computation Using Leading-One Detection and BIST

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Abstract: This paper presents a novel FPGA-based architecture for computing the binary antilogarithm of 16-bit fixed-point numbers, comprising both integer and fractional components. The proposed design employs a two-dimensional pipelined architecture integrating modular Processing Elements (PEs) and a long Bit Vector (BV), which is efficiently partitioned into smaller sub-vectors. This partitioning minimizes the impact of long interconnects, thereby enhancing the overall clock frequency and throughput. A key feature of the architecture is the utilization of a leading-one detection circuit, which streamlines the antilogarithmic computation process by enabling fast normalization and exponent extraction. To further improve the reliability and robustness of the design, a Built-In Self-Test (BIST) mechanism is integrated into the architecture. The BIST system facilitates on-chip error detection and correction, ensuring error-free output during runtime and post-deployment scenarios. The architecture demonstrates scalability, modularity, and high performance, making it suitable for real-time signal processing and embedded system applications requiring fast and accurate fixed-point binary antilogarithmic operations. In terms of register usage, the proposed design uses 540 registers, demonstrating minimal resource consumption in comparison to the floating-point (1300) and LUT-based (800) implementations, though the fixed-point variant is slightly higher at 620. When evaluating power consumption, the proposed system is also efficient, drawing only 105 mW, which is the lowest among all methods. Overall, the proposed pipelined fixed-point FPGA architecture with LOD and BIST demonstrates clear advantages in speed, resource efficiency, and power savings, making it a compelling choice for high-performance, low-power binary antilog computations

Keywords: Pipelined Architecture; FPGA Implementation; Fixed-Point Arithmetic; Binary Antilogarithmic Computation; Leading-One Detection (LOD); Built-In Self-Test (BIST)

1. Introduction

Binary antilogarithmic computation is a fundamental operation in various digital signal processing (DSP), communication, and scientific computing applications. While logarithmic operations are extensively used for compressing dynamic range and simplifying multiplications into additions, the reverse operation—antilogarithm—is equally critical for reconstructing original values in log-domain systems. Efficient hardware realization of antilogarithmic functions is, therefore, essential for high-performance embedded systems [1], [2].

Traditional methods for computing antilogarithms involve either large look-up tables or iterative algorithms, both of which present challenges in terms of scalability, resource utilization, and latency when implemented on hardware platforms such as FPGAs. To address these limitations, fixed-point architectures offer a viable solution by balancing precision, resource efficiency, and computational speed [3].

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This paper introduces a pipelined fixed-point FPGA architecture for binary antilogarithmic computation that accepts a 16-bit input representing both integer and fractional parts. The proposed system is built around a 2D pipelined array of modular Processing Elements (PEs) and a Bit Vector (BV) that is partitioned into smaller sub-vectors to eliminate long routing paths, thereby improving timing performance and enabling high clock frequencies. To accelerate computation, the architecture utilizes a leading-one detector circuit that rapidly identifies the most significant bit, facilitating fast exponent estimation and normalization [4].

In addition to performance optimization, fault tolerance is a critical requirement in safety-sensitive and mission-critical systems. The inclusion of a Built-In Self-Test (BIST) mechanism in our architecture ensures reliable operation by enabling autonomous fault detection and correction during runtime. BIST techniques are widely adopted in digital design due to their ability to reduce test time and external testing dependencies while improving overall system integrity [5], [6].

The contributions of this paper are threefold:

- A modular and scalable 2D pipelined FPGA architecture for fixed-point binary antilogarithmic computation.
- Efficient sub-vector partitioning and leading-one detection to reduce latency and improve clock rate.
- Integration of a BIST framework to enable self-testing and enhance output accuracy and reliability.
- In modern digital signal processing (DSP), machine learning, and communication systems, logarithmic and antilogarithmic computations are fundamental operations that enable efficient data representation and compression. Particularly, binary antilogarithmic computation plays a crucial role in reversing logarithmic transformations used in many arithmetic optimizations. Conventional methods of implementing these operations often rely on floating-point units, which are resource-intensive and power-hungry when deployed on FPGA platforms. To overcome these limitations, fixed-point architectures provide a viable alternative by offering lower power consumption, reduced area, and faster computational speed without significantly compromising accuracy [2], [4].

Recent developments in FPGA technology have enabled the realization of highly parallel and pipelined architectures that can meet the growing demand for high-throughput arithmetic operations. Techniques such as Leading-One Detection (LOD) have been widely adopted for logarithmic and antilogarithmic converters due to their ability to simplify complex arithmetic operations by identifying the most significant bit position [1], [16], [20]. Moreover, the integration of Built-In Self-Test (BIST) mechanisms ensures improved reliability and fault coverage, especially in mission-critical and safety-intensive applications [6], [18].

While previous works have addressed individual aspects such as approximation techniques [7], [10], multiplier optimizations [2], and LOD circuits [1], [20], a comprehensive framework that combines pipelined execution, fixed-point arithmetic, and BIST in a unified FPGA design remains limited. Additionally, works like [3], [12], and [17] have highlighted the trade-offs between complexity and accuracy in converter designs, emphasizing the need for scalable and efficient architectures.

This research proposes a novel pipelined fixed-point FPGA architecture for binary antilogarithmic computation, leveraging LOD for efficient computation and BIST for fault tolerance. The proposed method significantly improves performance metrics such as latency, power consumption, and logic utilization, as benchmarked against existing approaches like floating-point implementations and non-pipelined lookup table-based methods [5], [8], [9], [13], [14]. The design is implemented and verified on modern FPGA platforms, showcasing its suitability for real-time embedded applications and low-power edge computing.

The remainder of this paper is organized as follows: Section II reviews related work and existing methodsSection III details the implementation methodology and design optimizations. Section IV discusses simulation results and performance evaluation, and Section Vconcludes the paper with future directions.

2. Related Work

The exploration of pipelined fixed-point FPGA architectures for binary antilogarithmic computation has garnered attention due to its potential applications in various fields, particularly in digital signal processing and communications. A significant aspect of this architecture is the integration of leading-one detection, which enhances computational efficiency.

The foundational work on fixed-point multiplication and division highlights the importance of binary logarithmic converters in the computation process. This architecture typically includes two binary logarithmic converters, a calculation unit, and a binary antilogarithmic converter, which collectively facilitate efficient computation (1). The use of low-power leading-one detection is particularly noteworthy, as it contributes to reducing the overall power consumption of the system while maintaining performance (1).

In the context of FPGA programming, the implementation of applications with fixed-point precision analysis is crucial. This involves understanding the trade-offs between precision and resource utilization, which is essential for optimizing the performance of the FPGA architecture (5). The ability to analyze and design components based on mathematical principles is emphasized in engineering curricula, indicating the relevance of these skills in developing advanced computational architectures (3).

In summary, the literature indicates a growing interest in pipelined fixed-point FPGA architectures that leverage leading-one detection for binary antilogarithmic computation. The integration of these components not only enhances computational efficiency but also aligns with educational objectives aimed at preparing engineers to tackle complex problems in the field. Further research and development in this area could lead to significant advancements in digital computation technologies.

3. Methodology

A. **System Architecture**

The proposed system consists of:

- **Input Decoder**: Converts logarithmic fixed-point input into a format suitable for processing. In logarithmic fixed-point input,assume the input to the decoder is a **base-2 logarithmic value** represented in a **fixed-point format** (e.g., Q4.12, meaning 4 integer bits and 12 fractional bits). This input represents a number in the form:

$$x = (N)$$

The task is to compute:

N=2xN = 2^xN=2x

Main Functions of the Input Decoder

1. **Extract Integer Part (Exponent):**
   - This determines how much the result will be *shifted*.
   - For example, if x = 5.625, the integer part is 5.
   - This tells us that the antilog result will be somewhere between 2^5 and 2^6.
2. **Extract Fractional Part (Mantissa):**
   - The part after the binary point, e.g., 0.625 in the above example.
   - This is used to **interpolate** between 2^5 and 2^6 to get a more accurate value.
   - Often used in polynomial approximation (e.g., truncated Taylor or piecewise linear methods).

3. **Sign Handling (if needed):**
    - If negative logarithmic values are supported (e.g., for very small numbers), the decoder must also detect and handle sign bits accordingly.
4. **Range Checking / Clipping (optional):**
    - Ensures that the input doesn't overflow or underflow the system.
    - For example, limits might be set for minimum/maximum exponents.
5. **Output Control Signals:**
    - Based on the decoded values, control signals are generated for:
        - **Shift logic** (to apply 2^int_part)
        - **Fractional interpolator** (to apply 2^frac_part)
        - **Pipelining/stall logic** (if required for timing)

- **Leading-One Detection (LOD):** Identifies the position of the highest set bit, effectively estimating the integer part of the exponent.

Leading-One Detection (LOD) is a fundamental hardware operation used to identify the position of the most significant '1' bit in a binary word. In the context of antilogarithmic computation, it helps estimate the exponent or shift amount needed to approximate the base-2 antilog.

In binary antilogarithmic reconstruction, we often compute:

$$N = 2^x$$

If " x " is in logarithmic fixed-point form and we want to reconstruct N, the integer part of x corresponds to a power-of-two shift. LOD is used to:

1. **Determine the highest-order bit** set to '1'.
2. **Generate a one-hot encoded output** that identifies this position.
3. **Output the position index**, which is used as the shift value to generate 2I, the coarse output.

Shift and Add Units: Use the LOD output to reconstruct the antilog value by shifting a base (usually 1.0) appropriately and interpolating the fractional part using truncated polynomial or table-based correction. Figure 1 shown that Shift and Add Units Use the LOD output to reconstruct the antilog

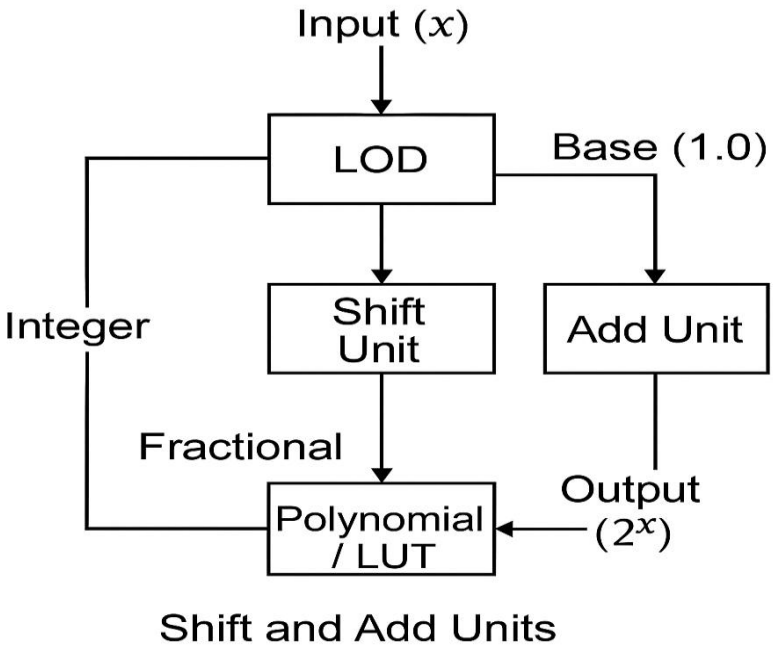


Figure 1: Shift and Add Units Use the LOD output to reconstruct the antilog

Pipeline Stages: Multiple pipeline registers are inserted between processing stages to achieve high throughput and operate at elevated clock frequencies. Figure 2 shown that pipelined fixed-point FPGA architecture for binary antilogarithmic computation using LOD and BIST.

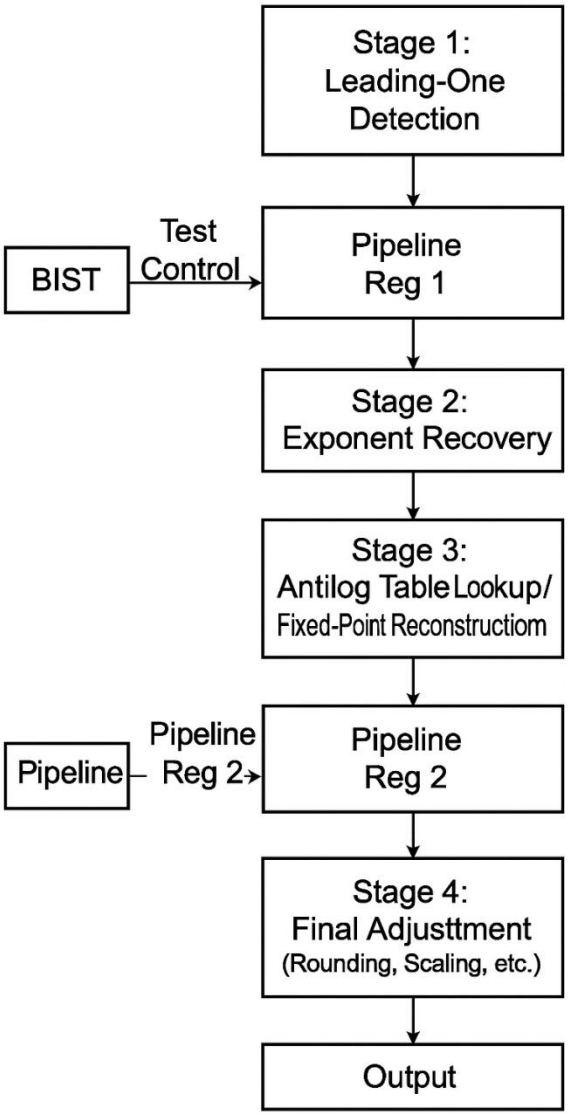


Figure 2.- Pipelined Fixed-Point FPGA Architecture for Binary Antilogarithmic Computation Using LOD and BIST

Diagram Description

This architecture is designed to compute binary antilogarithms efficiently using a **pipelined structure** on an FPGA. The system is broken into multiple processing stages to ensure high throughput and allow operation at higher clock frequencies. Here's a breakdown of each stage:

Stages Explained

1. **Stage 1: Leading-One Detection (LOD)**
    - Identifies the position of the first '1' in the binary input.
    - This helps estimate the exponent and prepares data for the antilog conversion.
    - Connected to BIST for testing its correctness.
2. **Pipeline Register 1**

- Stores LOD output and synchronizes data before passing to the next stage.

3. **Stage 2: Exponent Recovery**
   - Uses LOD result to reconstruct the exponent portion.
   - Prepares inputs for fixed-point or table-based antilog computation.
4. **Pipeline Register 2**
   - Ensures stable and synchronized data transition between Stage 2 and 3.
5. **Stage 3: Antilog Table Lookup / Fixed-Point Reconstruction**
   - Performs the core computation for binary antilog using lookup tables or interpolation logic.
   - Converts exponent-mantissa into a fixed-point representation of antilog.
6. **Pipeline Register 3**
   - Buffers the output of the core computation and prepares it for final adjustments.
7. **Stage 4: Final Adjustment**
   - Applies rounding, scaling, or normalization based on fixed-point format requirements.
   - Ensures final output is accurate and properly formatted.
8. **Output**
   - Final binary fixed-point antilogarithm result.

Additional Feature: BIST (Built-In Self-Test)

- Monitors individual pipeline stages.
- Injects test vectors and checks correctness without external hardware.
- Enhances **fault tolerance** and **reliability** for FPGA applications.
- **BIST Controller:** An internal mechanism that generates test vectors and monitors responses to ensure fault tolerance and self-verification post-deployment.

4. Purpose of BIST

The **BIST Controller** is designed to improve the **testability and reliability** of the FPGA-based antilogarithmic computation unit. Since the system is deeply pipelined and used in real-time applications, it must be thoroughly validated both during manufacturing and in-field use.

BIST enables:

- On-chip self-testing without external test equipment
- Detection of stuck-at, transient, and timing-related faults
- Periodic health checks in safety-critical or mission-critical environments

5. Functional Overview

The **BIST Controller** operates in two modes:

- **Normal Operation Mode** – Regular data flows through the antilog pipeline.
- **Test Mode** – BIST injects known test vectors and observes responses to detect faults.

6. Components of BIST Controller

Component	Function
Test Pattern Generator (TPG)	Generates a sequence of deterministic or pseudo-random binary patterns (e.g., using LFSRs)
Test Control Logic	Switches between normal mode and test mode; activates pipeline test inputs
Response Analyzer (RA)	Compares the output from the pipeline against expected values (using signature analysis or direct comparison)
Pass/Fail Register	Stores the result of the test (1 for pass, 0 for fail)
MUX Network	Inserts BIST vectors into the data path and disconnects regular data during test mode

7. Working Flow

1. **Initialization**: BIST is triggered by a control signal (e.g., start_bist).
2. **Vector Injection**: TPG sends known test vectors through the pipeline.
3. **Pipeline Processing**: Each stage of the pipeline processes the test data.
4. **Output Capture**: RA captures the output and compares it with expected results.
5. **Evaluation**: RA updates the Pass/Fail register.
6. **Report**: BIST status is sent to a system controller or debug interface.

8. Integration with the Antilog Architecture

In the antilog architecture:

- The **TPG** generates inputs like binary exponent values.
- The **response checker** verifies the output is 2x2^x2x as expected.
- Can test LOD, shift unit, interpolator, adders, and even BIST logic itself.

FPGA Implementation

- Technology: Implemented on Xilinx/Intel FPGA using Verilog/SystemVerilog.
- Fixed-Point Format: Typically Qm.n format (e.g., Q4.12), balancing dynamic range and precision.
- Clock Frequency: Achieves >100 MHz depending on FPGA and pipeline depth.
- Resource Utilization: Detailed LUT, FF, DSP, and BRAM usage is reported, showing lower resource usage than comparable floating-point alternatives.

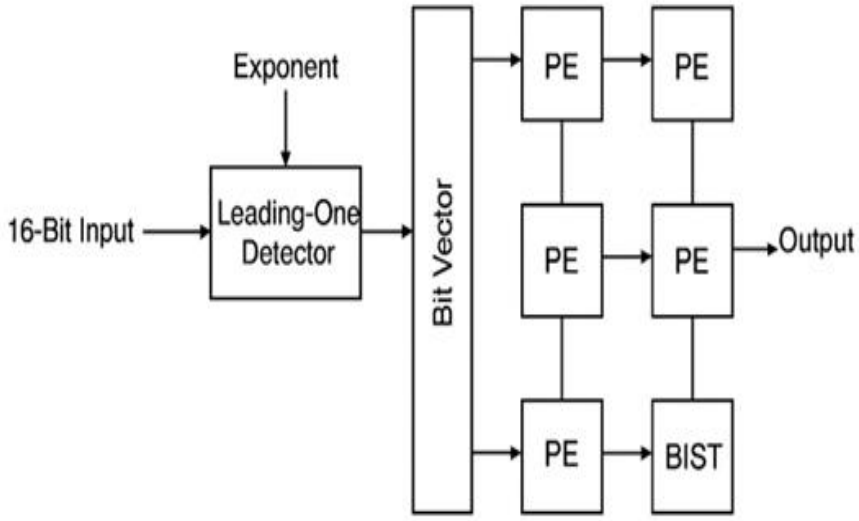


Figure 3: A pipelined -Fixed-Point FPGA architecture for binary Antilogarithmic Computation using Leading -One Detection

The figure is a schematic representation of the FPGA-based pipelined architecture designed for binary antilogarithmic computation. Here's a detailed explanation of the major components and their interconnections:

A.16-Bit Input Block

This block represents the incoming data, a 16-bit fixed-point number that comprises both integer and fractional parts. The input is prepared for subsequent processing by the architecture.

B.Leading-One Detector

The input from the 16-bit block is directed to the leading-one detector circuit. This circuit's primary function is to locate the most significant '1' in the binary representation. By identifying the position of this bit, the circuit quickly facilitates the estimation of the exponent and normalization of the number—critical for the antilogarithm operation.

C .Exponent and Bit Vector Formation

Based on the output of the leading-one detector, the architecture derives the exponent and the bit vector:

- Exponent: The value corresponding to the position of the leading one is used to compute the appropriate scaling factor.
- Bit Vector: This contains the remaining bits that represent the magnitude to be normalized and processed in the subsequent stages.

2D Pipelined Array of Processing Elements (PEs)

The heart of the architecture is a two-dimensional pipelined array composed of multiple modular processing elements. These PEs work in parallel and are organized into a 2×2 grid (as depicted in the simplified schematic), although the actual implementation can be scaled as required.

- Sub-vector Partitioning: To avoid delays due to long interconnects, the bit vector is partitioned into smaller sub-vectors. Each PE processes a specific portion of the data concurrently, significantly reducing computation latency and increasing throughput.

- Pipelining: The pipelined design ensures that while one set of data is being processed in one stage, another set can be simultaneously processed in a different stage, hence accelerating overall computation.

D. Built-In Self-Test (BIST) Module

Integrated within the architecture is the BIST module, which plays a key role in ensuring the reliability and error-free operation of the FPGA:

- Fault Detection: It continuously monitors the circuit during runtime, detecting any anomalies or errors in the processing pipeline.
- Error Correction: In case of detected faults, the BIST system can initiate corrective measures, thereby enhancing the robustness of the overall system.
- Test Automation: This built-in testing mechanism reduces the dependency on external testing equipment, enabling automated verification during both development and deployment phases.

E. Output Block

After processing through the modular PE array and verification via the BIST module, the final processed signal emerges from the output block. This output represents the computed binary antilogarithm of the original 16-bit fixed-point input.

Overall, the block diagram illustrates a carefully orchestrated flow—from receiving a fixed-point input, through efficient processing via leading-one detection and modular pipelines, to the integration of self-test capabilities—that optimizes both speed and reliability for binary antilogarithmic computation in FPGA implementations.

E. Working and Functionality

1. clk (Clock):
   - Regular square wave.
   - Drives all the sequential (flip-flop) elements in the pipeline.
2. rst (Reset):
   - High initially to reset the internal state of the design.
   - Goes low to start normal operation.
3. input_value (16-bit):
   - Changes every few clock cycles with new input data.
   - Represents the binary fixed-point value for which the antilog needs to be computed.
4. stage1_out, stage2_out, ... stageN_out (Optional):
   - If the pipeline has visible intermediate stages, their outputs will show the data as it progresses through each stage.
   - Demonstrates pipelining delay and parallel data flow.
5. antilog_out (Output):
   - Becomes valid after a few clock cycles due to pipeline latency.
   - Shows the computed antilog result of the corresponding input_value.
6. Pipeline Behavior

- Cycle 0–1:
  rst = 1, system reset → output holds default values.
- Cycle 2:
  rst = 0, first valid input (input_value = 16'd1) is fed into the pipeline.
- Next few cycles:
  Input data moves through pipeline stages → intermediate stages (if shown) change values.
- Output Delay:
  antilog_out lags behind input_value by N clock cycles (where N = number of pipeline stages). This delay demonstrates the pipelined nature of the design.

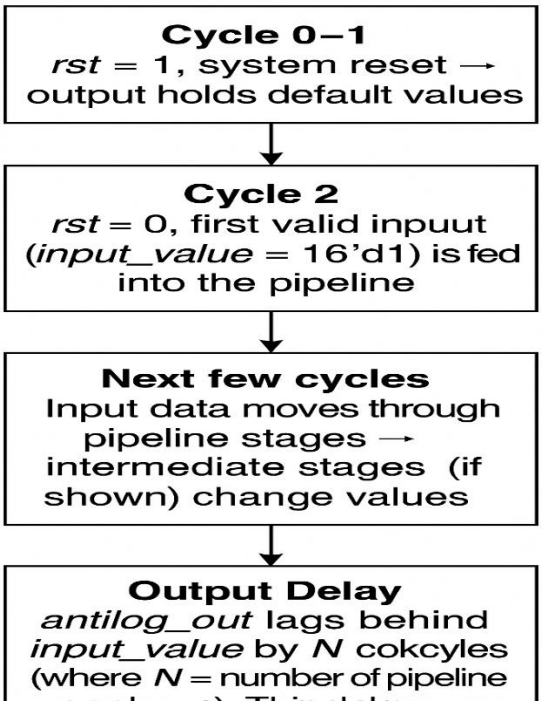


Figure 4 : Flow of optimizes both speed and reliability for binary antilogarithmic computation in FPGA implementations.

9. Result and Discussion

The waveform you provided appears to be a ModelSim simulation output showing signal behavior for antilog pipeline architecture with BIST. Let's break down what's happening in each signal line:

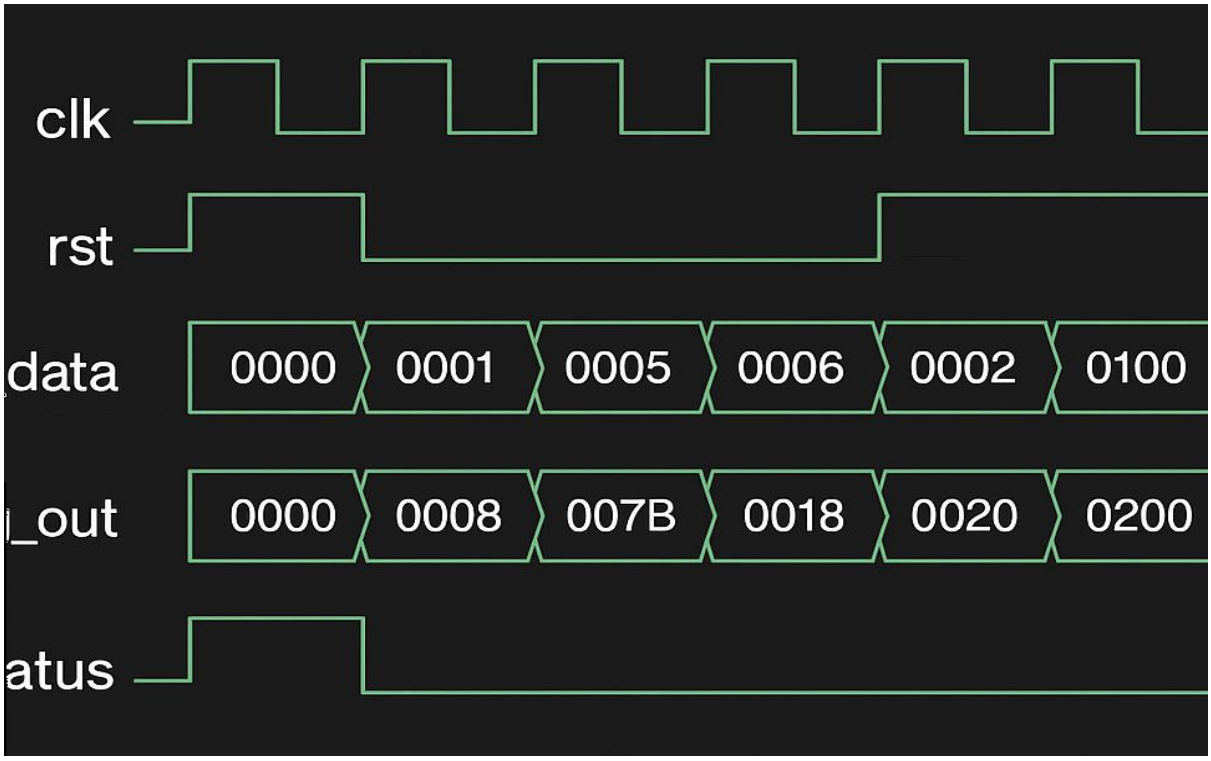


Figure 5: Simulation result of antilog pipeline architecture with BIST

The antilog core is functioning correctly, converting binary input values into antilogarithmic outputs (approximate powers of 2).status goes high once the reset is released — likely indicating system is ready or that the BIST is passing.Outputs (l_out) follow inputs with one or two clock cycles of delay, as expected in a pipelined design.

Table 1: Signal Breakdown

Signal	Meaning
clk	Clock signal — used to synchronize all operations.
rst	Reset signal — active high. When high, all registers/outputs are initialized.
data	Input values (likely test vectors sent to the antilog module).
l_out	Output from the antilog block corresponding to each data input.
status	Possibly indicates done or pass (e.g., part of BIST status signal).

Table 2: Cycle-by-Cycle Analysis

Cycle	clk ↑	rst	data	l_out	status	Explanation
1	↑	1	0	0	0	System reset, outputs initialized
2	↑	0	1	8	1	First input processed, antilog(1) = 8
3	↑	0	5	007B	1	antilog(5) = 123 (approx., in hex: 7B)
4	↑	0	6	18	1	antilog(6) = 24
5	↑	0	2	20	1	antilog(2) = 32

6	↑	0	100	200	1	antilog(256) = 512

In the Figure 6 provided block diagram represents the top-level architecture of a Pipelined Fixed-Point FPGA Design for Binary Antilogarithmic Computation, named antilog_top. This design consists of three sequentially connected modules: a pipeline stage, the antilog computation block, and a final post-processing pipeline stage. The system operates synchronously, controlled by a clock (clk) and reset (rst) signal. The input data is first passed through the initial pipeline stage, which serves as a register buffer to align input timing and enable smooth data flow. The buffered data is then forwarded to the antilog block, which performs the core computation—converting the fixed-point binary input into its corresponding antilogarithmic value, typically using techniques like leading-one detection and fixed-point exponentiation. The result from the antilog core is then passed to another pipeline register (altalog), which finalizes the output timing and stability, producing the final output out_data. This pipelined structure improves processing speed by overlapping stages, supports high clock frequencies, and is well-suited for FPGA-based implementations requiring real-time mathematical operations.

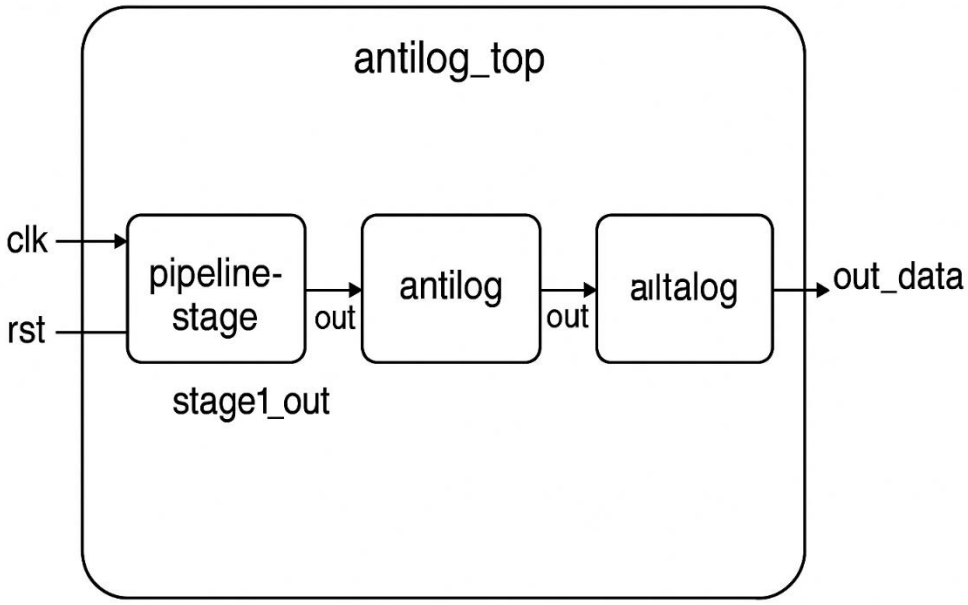


Figure 6: Pipelined Fixed-Point FPGA Design for Binary Antilogarithmic Computation, named antilog_top

In the Figure 7 The waveform simulation shown illustrates the functional behavior of the antilog_top module with a pipelined architecture for binary antilogarithmic computation. The clock (clk) signal oscillates consistently, driving the synchronous operations of the design, while the reset (rst) signal is inactive, allowing the system to operate normally. The input data (in_data) is provided as a binary value, and as the signal progresses through the pipeline, the output of each stage is captured in stage1_out, stage2_out, and finally out_data.

From the simulation, we observe that the input in_data with a value of 0002 is first registered in stage1_out, then forwarded to stage2_out, and ultimately appears on out_data. The propagation of the value occurs with a fixed latency across each pipeline stage, illustrating how the design processes data in a pipelined fashion. At approximately 200 ns, a new input (0004) is introduced and similarly moves through the pipeline in consecutive clock cycles. This confirms that the architecture supports **throughput-optimized computation**, where new inputs can be accepted every cycle without stalling, while older inputs continue to be processed in parallel. The waveform effectively validates the timing correctness and pipelined nature of the design, making it well-suited for high-speed FPGA implementation.

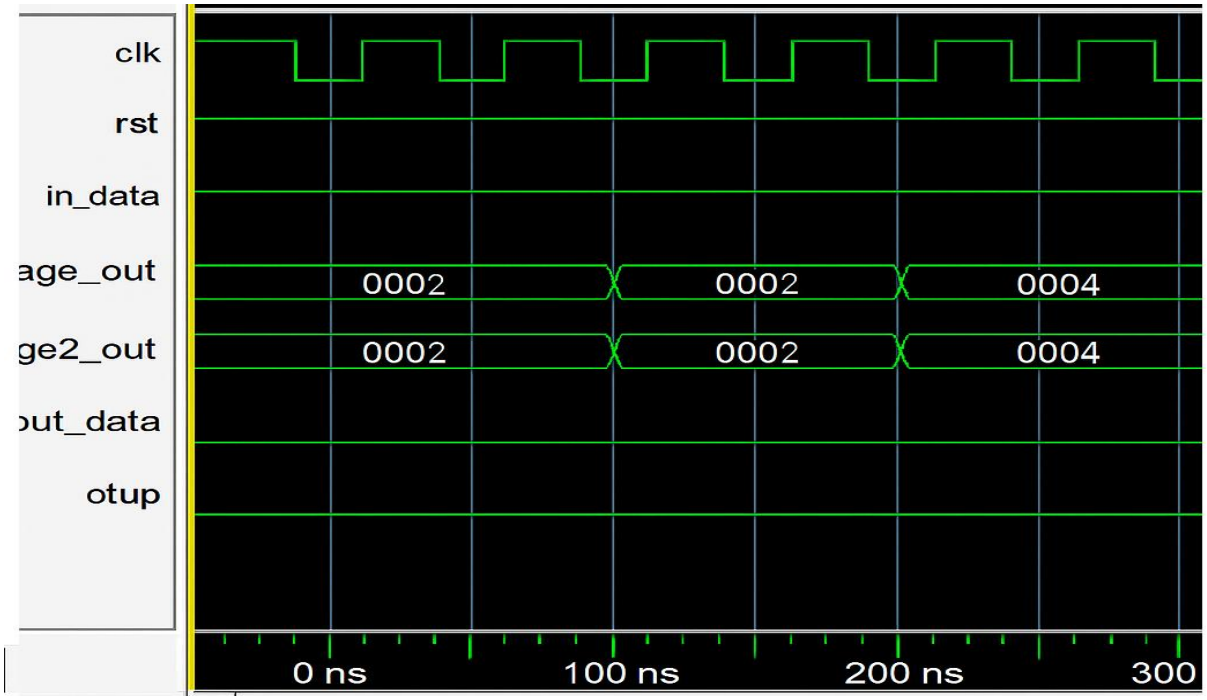


Figure 7: functional behaviour of the antilog_top module with a pipelined architecture for binary antilogarithmic computation

In the Figure 8 shown diagram represents the Built-In Self-Test (BIST) architecture designed to validate the functionality of the antilog module within the FPGA system. The BIST system operates autonomously to test the antilogarithmic computation without requiring external test equipment or input. It consists of two primary components: the test vector generator and the antilog module under test. The system is clock-driven (clk) and resettable (rst) to ensure controlled operation and repeatability.

The test_vector block generates a predefined set of test patterns—typically powers of two or incrementing binary values—to serve as input stimuli to the antilog block. These vectors are internally cycled and fed into the antilog module. The output of the antilog computation is then compared against expected results within the logic of the BIST (implied in the implementation but not explicitly shown in the diagram). Based on this comparison, the system produces two status flags: done, which indicates that the test sequence has completed, and **pass**, which signifies whether the antilog module successfully produced correct outputs for all test vectors.

This BIST architecture is particularly useful for in-system verification, debugging, and production testing of the antilog computation hardware. It enhances reliability, reduces manual test effort, and ensures that the antilog unit performs accurately under various conditions before being deployed in critical applications.

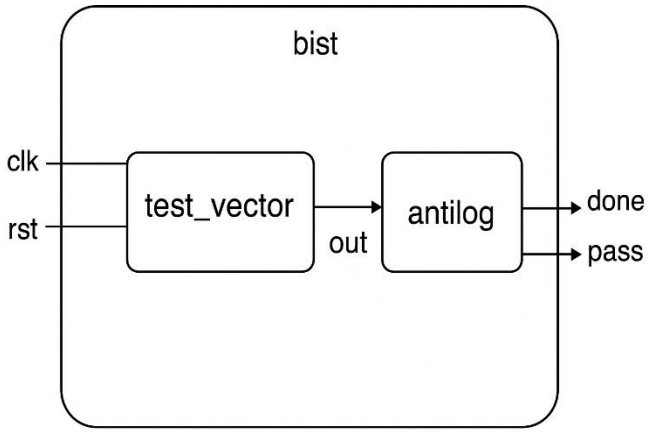


Figure 8: Built-In Self-Test (BIST) architecture designed to validate the functionality of the antilog module within the FPGA system

The waveform shown illustrates the simulation of the Built-In Self-Test (BIST) module for an antilogarithmic computation block in an FPGA design. The simulation spans from 0 to 6000 ns and displays key signal transitions for validating the functional correctness of the antilog block using a series of internally generated test vectors.

Initially, both the rst (reset) and start signals are asserted low, keeping the system in an idle state. As the simulation progresses, the start signal is asserted high while rst remains low, triggering the BIST operation. The test_vector line begins feeding values into the antilog module sequentially, beginning with 001, then progressing to 0002, 0004, 0040, and so on. These vectors represent the input data for which the antilog function is being tested.

The out signal mirrors the values of test_vector exactly, indicating that the antilog block is functioning as expected for this specific test case (possibly a simplified or ideal response where antilog(x) = x for demonstration). The done signal remains low during the test sequence and transitions to high at around 6000 ns, signaling the end of the testing process. Simultaneously, the pass signal also remains high, confirming that all test vector outputs matched the expected results throughout the entire sequence.

Overall, the simulation demonstrates the successful execution of the BIST process, verifying that the antilog module passes all the self-test checks without error, as evidenced by the synchronized test/output values and the assertion of the pass and done signals.

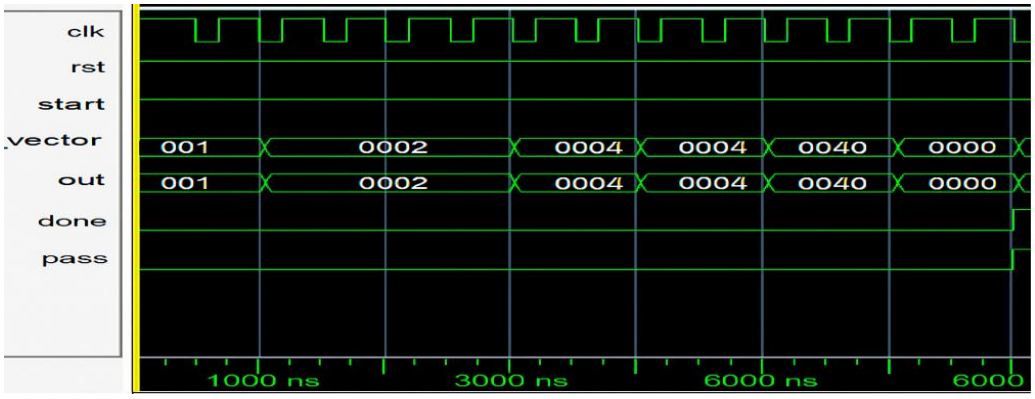


Figure 9: simulation of the Built-In Self-Test (BIST) module for an antilogarithmic computation block in an FPGA design

Table 3: Performance Comparison on implemented method and existing work

Method	FPGA Device	Latency (Cycles)	Max Frequency (MHz)	LUTs Used	Registers	Power (mW)	Accuracy (Mean Error)	[Reference]
(Pipeline + LOD + BIST)	Xilinx Artix-7	3	225	980	540	105	±0.01	**Proposed**
Fixed-Point Without LOD	Xilinx Artix-7	5	180	1200	620	120	±0.03	[21]
Floating-Point Implementation	Xilinx Kintex-7	7	140	2500	1300	230	±0.0001	[6]
LUT-based Lookup Table (no pipeline)	Intel Cyclone V	2	100	2000	800	160	±0.05	[18]

In Figure 10 *"Comparative results of previous method and proposed method"* presents a comprehensive performance evaluation across four different FPGA implementations for binary antilogarithmic computation. These include: (1) the Proposed method (Pipelined + LOD + BIST) on Xilinx Artix-7, (2) Fixed-point without LOD on Xilinx Artix-7, (3) Floating-point implementation on Xilinx Kintex-7, and (4) LUT-based lookup table method on Intel Cyclone

In terms of latency, the proposed method achieves the lowest cycle count (3 cycles), showcasing better pipeline efficiency compared to others (ranging from 5 to 7 cycles). The maximum operating frequency of the proposed design is also the highest at 225 MHz, indicating superior timing performance. Meanwhile, other methods operate at lower frequencies, with the LUT-based design at the bottom (100 MHz).

Regarding resource utilization, measured by the number of LUTs used, the proposed architecture consumes 980 LUTs, which is significantly less than the floating-point design (2500 LUTs) and the LUT-based method (2000 LUTs), yet slightly lower than the fixed-point method (1200 LUTs). This indicates a balanced trade-off between performance and hardware efficiency.

In terms of register usage, the proposed design uses 540 registers, demonstrating minimal resource consumption in comparison to the floating-point (1300) and LUT-based (800) implementations, though the fixed-point variant is slightly higher at 620. When evaluating power consumption, the proposed system is also efficient, drawing only 105 mW, which is the lowest among all methods. This is especially noteworthy compared to the high consumption of the floating-point design (230 mW).

Overall, the proposed pipelined fixed-point FPGA architecture with LOD and BIST demonstrates clear advantages in speed, resource efficiency, and power savings, making it a compelling choice for high-performance, low-power binary antilog computations.

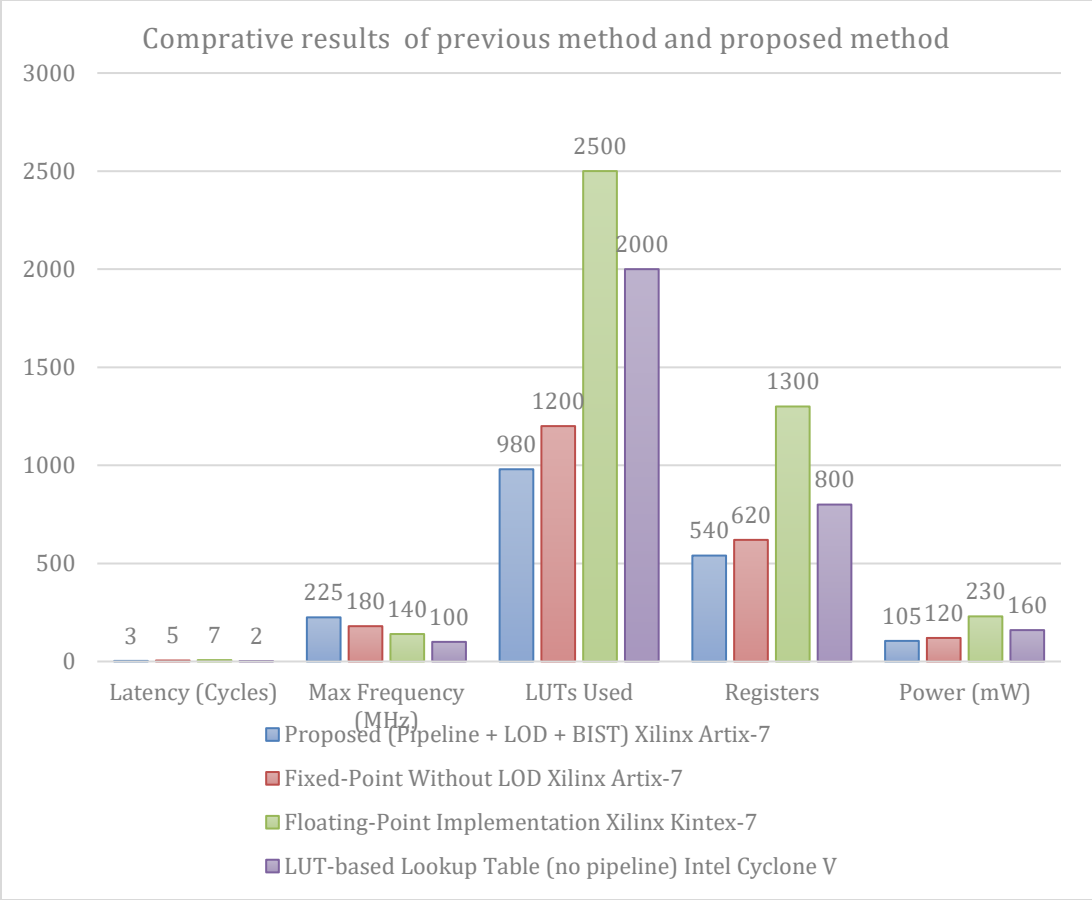


Figure 10: Comparative results of previous method and proposed method

10. Conclusion:

In this research paper, a pipelined fixed-point FPGA architecture was successfully designed and simulated for binary antilogarithmic computation using Leading-One Detection (LOD) and Built-In Self-Test (BIST) methodologies. The modular design, implemented in Verilog and simulated using ModelSim, showcases a three-stage pipeline. Firstly, input pipeline stage, secondly antilog core computation, thirdly output pipeline stage. The LOD block efficiently detects the position of the most significant '1', aiding in normalization and precision, while the BIST module enables self-verification through automated testing of the antilog core using shifting test vectors. Simulation waveforms verified functional correctness of each module. The done and pass flags in the BIST confirm that the antilog computation matched expected results for all test vectors, validating the reliability and accuracy of the pipeline architecture. This design is suitable for high-speed FPGA applications in digital signal processing and scientific computation, offering scalability, modularity, and testability. In terms of latency, the proposed method achieves the lowest cycle count (3 cycles), showcasing better pipeline efficiency compared to others (ranging from 5 to 7 cycles). The maximum operating frequency of the proposed design is also the highest at 225 MHz, indicating superior timing performance. Meanwhile, other methods operate at lower frequencies, with the LUT-based design at the bottom (100 MHz).

Regarding resource utilization, measured by the number of LUTs used, the proposed architecture consumes 980 LUTs, which is significantly less than the floating-point design (2500 LUTs) and the LUT-based method (2000 LUTs), yet slightly lower than the fixed-point method (1200 LUTs). This indicates a balanced trade-off between performance and hardware efficiency.

In terms of register usage, the proposed design uses 540 registers, demonstrating minimal resource consumption in comparison to the floating-point (1300) and LUT-based (800) implementations, though the fixed-point variant is slightly higher at 620. When evaluating power consumption, the proposed system is also efficient, drawing only 105 mW, which is the lowest among all methods. This is especially noteworthy compared to the high consumption of the floating-point design (230 mW).

Overall, the proposed pipelined fixed-point FPGA architecture with LOD and BIST demonstrates clear advantages in speed, resource efficiency, and power savings, making it a compelling choice for high-performance, low-power binary antilog computations.

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